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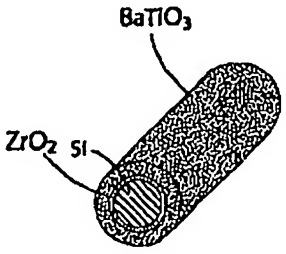
(54) Title: NANOSCALE WIRE-BASED DATA STORAGE



(57) Abstract: The present invention generally relates to nanotechnology and submicroelectronic devices that can be used in circuitry and, in some cases, to nanoscale wires and other nanostructures able to encode data. One aspect of the invention provides a nanoscale wire or other nanostructure having a region that is electrically-polarizable, for example, a nanoscale wire may comprise a core and an electrically-polarizable shell. In some cases, the electrically-polarizable region is able to retain its polarization state in the absence of an external electric field. All, or only a portion, of the electricallypolarizable region may be polarized, for example, to encode one or more bits of data. In one set of embodiments, the electrically-polarizable region comprises a functional oxide or a ferroelectric oxide material, for example, $BaTiO_3$, lead zirconium titanate, or the like. In some embodiments, the nanoscale wire (or other nanostructure) may further comprise other materials, for example, a separation region separating the electricallypolarizable region from other regions of the nanoscale wire. For example, in a nanoscale wire, one or more intermediate shells may separate the core from the electricallypolarizable shell.

NANOSCALE WIRE-BASED DATA STORAGE

RELATED APPLICATIONS

This application claims the benefit of U.S. Provisional Patent Application Serial No. 60/633,733, filed December 6, 2004, entitled "Nanoscale Wire Based Data Storage," by Lieber, et al., which is incorporated herein by reference.

FEDERALLY SPONSORED RESEARCH

Various aspects of the present invention were sponsored by DARPA, Grant Nos. N-00014-01-1-0651 and N00014-04-1-0591. The U.S. Government may have certain rights in the invention.

FIELD OF INVENTION

The present invention generally relates to nanotechnology and sub-microelectronic devices that can be used in circuitry and, in particular, to nanoscale wires and other nanostructures able to encode data.

BACKGROUND

Interest in nanotechnology, in particular sub-microelectronic technologies such as semiconductor quantum dots and nanowires, has been motivated by the challenges of chemistry and physics at the nanoscale, and by the prospect of utilizing these structures in electronic, optical, and related devices. While nanoscopic articles might be well-suited for transport of charge carriers and excitons (e.g. electrons, electron-hole pairs, electron pairs, etc.) and thus may be useful as building blocks in nanoscale electronics, optics, and other applications, much of nanotechnology and nanoelectronics is not well-developed. Thus there is a need in the art for new and improved articles and techniques involving nanoscale devices.

SUMMARY OF THE INVENTION

The present invention generally relates to nanoscale wires and other nanostructures, including those able to encode data. The subject matter of the present invention involves, in some cases, interrelated products, alternative solutions to a particular problem, and/or a plurality of different uses of one or more systems and/or articles.

In one aspect, the invention provides an electronic data storage device. According to one set of embodiments, the device includes a first electrode, a second electrode, a semiconductive material defining an electrical pathway between the first and second electrodes, and a material proximate the semiconductive material, switchable between at least a first polarization state and a second polarization state. In one embodiment, the semiconductive material is switchable between a first conductive state and a second conductive state in response to the first or second polarization states of the ferroelectric material, respectively, providing conductivity between the first and second electrodes, respectively, of a first conductivity and a second conductivity at least 1000 times the first conductivity.

The electronic data storage device, in another set of embodiments, includes a first electrode, a second electrode, and a semiconductive material defining an electrical pathway between the first and second electrodes. In one embodiment, the semiconductive material includes at least a first switch region and a second switch region along the electrical pathway, each of the first and second switch regions separately and independently switchable between a first conductive state and a second conductive state, which second state provides conductivity along the electrical pathway in the respective region at least 1000 times that of first state in the respective region.

In yet another set of embodiments, the electronic data storage device includes a semiconductive data storage element having an off state, and an on state providing electrical conductivity at least 1000 times that of the off state. The data storage element may have a write voltage able to switch the element from the on state to the off state and/or vice versa, and a read voltage through which the state of the element can be determined. In certain embodiments, the read and write voltages differ by no more than 1 or 2 V.

The invention, according to another aspect, is an article. In one set of embodiments, the article includes a first electrode, a second electrode, a semiconductive material defining an electrical pathway between the first and second electrodes, and at least two control terminals, each in electrical communication with the semiconductive material along the electrical pathway between the first and second electrodes.

The article, in another set of embodiments, includes a nanoscale wire comprising an electrically-polarizable region. The electrically-polarizable region, in one

embodiment, is able to retain its polarization state in the absence of an electric field. The article, according to still another set of embodiments, includes a nanoscale wire comprising a core and a shell at least partially surrounding the core. In one embodiment, the core is semiconductive or conductive. In some cases, the shell includes a ferroelectric oxide material.

In yet another set of embodiments, the article includes a device comprising an array of nonvolatile memory elements. The article, in one embodiment, includes a plurality of memory elements each comprising a nanoscale wire comprising a transistor architecture. In still another set of embodiments, the article includes a nanoscale wire comprising a core and at least two shells, where each shell surrounding at least a portion of the core. The nanoscale wire comprises a ferroelectric oxide material in one embodiment. In another set of embodiments, the article includes a nanoscale wire comprising a transistor architecture. The nanoscale wire comprises a ferroelectric oxide material, in at least one embodiment. In yet another set of embodiments, the article includes a nanoscale wire comprising a core and a shell, where the nanoscale wire comprises Ba. The article, in still another set of embodiments, includes a nanoscale wire comprising a core and at least two shells, where at least one of the shells has a dielectric constant of at least about 15.

In one set of embodiments, the article comprises a nanoscale wire encoding more than one bit of data. According to another set of embodiments, the article includes a nanoscale wire comprising a region encoding a bit of data, where the region is not defined by the position of a second, movable nanoscale wire.

The article includes a device comprising an array of memory elements in one set of embodiments, each having an area of less than about 20 nm^2/bit. According to yet another set of embodiments, the article includes a memory element having a reading voltage of less than about 1 $V_{absolute}$ at an on/off current differential ratio of at least 1000. The article, in still another set of embodiments, includes a memory element having a writing voltage of less than about 1 $V_{absolute}$ at an on/off current differential ratio of at least 1000. In yet another set of embodiments, the article includes a memory element having a read/write voltage ratio of less than about 1:1.5 at an on/off current differential ratio of at least 1000. The article includes a memory element having a first stable state having a first conductivity and a second stable state having a second conductivity, in still

another set of embodiments, where the first conductivity is at least 1000 times greater than the second conductivity.

In yet another aspect, the invention provides a method. The method, in one set of embodiments, includes an act of polarizing, in a nanoscale wire comprising a core and a shell, at least a portion of the shell.

One set of embodiments provides a method comprising acts of encoding a first bit of data on a nanoscale wire, and encoding a second bit of data on the nanoscale wire without substantially altering the first bit of data. In another set of embodiments, the method includes acts of reading a first bit of data from a nanoscale wire, and reading a second bit of data, independent of the first bit, from the nanoscale wire. The method, in yet another sets of embodiments, includes an act of encoding at least one bit of data in an immobile nanoscale wire.

In another set of embodiments, the method includes acts of providing a source electrode, a drain electrode, and a semiconductive material in electrical communication with both the source and drain electrodes, and independently writing and reading at least two separate bits of data in the semiconductive material.

Yet another set of embodiments provides a method including an act of depositing a ferroelectric oxide material on at least a portion of a nanoscale wire comprising a core and a first shell to form a second shell different from the first shell. In another set of embodiments, the method includes an act of depositing a ferroelectric oxide material on at least a portion of a nanoscale wire not immobilized to a substrate. Still another set of embodiments provides a method including an act of depositing a material having a dielectric constant of at least about 15 on at least a portion of a nanoscale wire not immobilized to a substrate.

In another aspect, the present invention is directed to a method of making one or more of the embodiments described herein. In yet another aspect, the present invention is directed to a method of using one or more of the embodiments described herein.

Other advantages and novel features of the present invention will become apparent from the following detailed description of various non-limiting embodiments of the invention when considered in conjunction with the accompanying figures. In cases where the present specification and a document incorporated by reference include conflicting and/or inconsistent disclosure, the present specification shall control. If two

or more documents incorporated by reference include conflicting and/or inconsistent disclosure with respect to each other, then the document having the later effective date shall control.

BRIEF DESCRIPTION OF THE DRAWINGS

Non-limiting embodiments of the present invention will be described by way of example with reference to the accompanying figures, which are schematic and are not intended to be drawn to scale. In the figures, each identical or nearly identical component illustrated is typically represented by a single numeral. For purposes of clarity, not every component is labeled in every figure, nor is every component of each embodiment of the invention shown where illustration is not necessary to allow those of ordinary skill in the art to understand the invention. In the figures:

Figs. 1A-1F illustrate various physical properties of certain nanoscale wires of an embodiment of the invention;

Fig. 2 illustrates the polarization of a nanoscale wire, in accordance with another embodiment of the invention;

Figs. 3A-3G illustrate a nanoscale wire able to encode more than one bit of data, according to yet another embodiment of the invention;

Figs. 4A-4C are schematic diagrams illustrating various embodiments of the invention;

Figs. 5A-5C are schematic diagrams illustrating the fabrication of electrodes suitable for use with certain embodiments of the invention;

Figs. 6A-6B are schematic diagrams illustrating various properties of certain nanoscale wire devices, according to an embodiment of the invention;

Figs. 7A-7D illustrate various memory architectures, useful in certain embodiment of the invention;

Figs. 8A-8C illustrate an example of a memory architecture using certain nanoscale wires of the invention, according to yet another embodiment;

Fig. 9A-9E illustrate certain nanoscale wires of an embodiment of the invention;

Figs. 10A-10F illustrate the use of certain nanoscale wires to store bits of data, according to another embodiment of the invention;

Fig. 11 illustrates a method of fabricating certain nanoscale wires of the invention, according to yet another embodiment;

Figs. 12A-12J illustrate certain nanoscale wires of the invention, according to still another embodiment;

Figs. 13A-13C illustrate 2DFT plots of certain nanoscale wires according to another embodiment of the invention;

Figs. 14A-14G illustrate various electrical characteristics of certain nanoscale wires of the invention, in another set of embodiments;

Figs. 15A-15B illustrate certain response limits of instruments used to measure properties of certain nanoscale wires of the invention;

Figs. 16A-16F illustrate various devices of the invention, having different gate widths, in another set of embodiments of the invention; and

Figs. 17A-17E illustrate certain devices of the invention, having multiple gates, in accordance with another embodiment of the invention.

DETAILED DESCRIPTION

The present invention generally relates to nanotechnology and sub-microelectronic devices that can be used in circuitry and, in some cases, to nanoscale wires and other nanostructures able to encode data. One aspect of the invention provides a nanoscale wire or other nanostructure having a region that is electrically-polarizable, for example, a nanoscale wire may comprise a core and an electrically-polarizable shell. In some cases, the electrically-polarizable region is able to retain its polarization state in the absence of an external electric field. All, or only a portion, of the electrically-polarizable region may be polarized, for example, to encode one or more bits of data. In one set of embodiments, the electrically-polarizable region comprises a functional oxide or a ferroelectric oxide material, for example, $BaTiO_3$, lead zirconium titanate, or the like. In some embodiments, the nanoscale wire (or other nanostructure) may further comprise other materials, for example, a separation region separating the electrically-polarizable region from other regions of the nanoscale wire. For example, in a nanoscale wire, one or more intermediate shells may separate the core from the electrically-polarizable shell.

One aspect of the invention provides a nanoscale wire having a core and a shell, where the shell comprises a functional oxide, and/or a ferroelectric oxide material such as a barium titanate (e.g., $BaTiO_3$), for example, as shown in Fig. 4A with nanoscale wire 5 having a core 10 and shell 20. One or more portions of shell 20 at least partially

surrounding at least a portion of the core may be independently polarized by applying an electric field 50 to that portion, and such portion(s), after polarization, may be able to retain the polarization state, even in the absence of an external electric field. The core may be electrically conductive (i.e., able to pass an electric current therethrough), and can be used to apply the electric field to the shell. For example, the core may comprise a semiconductor such as silicon, or a conductor. Other examples of semiconductors include elemental semiconductors, Group IV semiconductors, Group III-Group V semiconductors, Group II-Group IV semiconductors, or the like, as well as semiconductors having different levels of doping. Additional examples are further described below. Thus, it should be noted that the present invention is not confined to p-type doped silicon, but is applicable to other types of semiconductive materials with different types and/or levels of doping as well.

In certain embodiments, such nanoscale wires are useful in devices such as nonvolatile memory devices. More than one bit of data may be encoded within the nanoscale wire in some cases, for example, within different portions of a shell that have been independently polarized. Data (i.e., bits) can be encoded within a portion of the shell by applying an electric field to that portion (e.g., using a "writing voltage"). For example, the wire may be polarized by creating a first voltage gradient between the portion of the shell and the core (e.g., representing a "1"), and depolarized by creating a second voltage gradient, which may be smaller or negative with respect to the first voltage gradient, between the portion of the shell and the core (e.g., representing a "0"). Upon removal of the voltage gradient, the portion of the shell is able to retain its polarization state, in some cases, for at least hours, days, weeks, or longer. Without wishing to be bound by any theory, in some cases, due to the "binary" nature of the electrically-polarizable region at the quantum scale (e.g., an "up" electric dipole moment and a "down" electric dipole moment), the portion of the shell is able to retain its polarization state for very long periods of time without any appreciable decay or "leakage," as the quantum state of the portion of the electrically-polarizable region (e.g., an "up" electric dipole moment and a "down" electric dipole moment) prevents substantial leakage or intermediate values, and the nanoscale dimensions of the nanoscale wire allow the electrically-polarizable region to control the conductivity and/or other electrical properties of the nanoscale wire, as discussed herein. It should be noted

that the designations of "1" for a polarized state and "0" for a depolarized or an oppositely polarized state are arbitrarily chosen, and that, in another embodiment of the invention, "0" may be chosen for a polarized state and "1" for a depolarized or an oppositely polarized state. With the benefit of the present disclosure, those of ordinary skill in the art will know of suitable techniques to read/write data to a nanoscale wire using any polarization encoding scheme.

In one embodiment, a polarized shell may change the conductance of the core proximate (i.e., in contact, or at least near) the polarized region with respect to an unpolarized shell, and higher amounts of polarization can have correspondingly greater effects on the conductivity in some cases (other embodiments are discussed in more detail, below). Thus, the polarization state of the shell may be determined by measuring the conductance of the core. For example, if the core comprises p-type doped silicon, a polarization state in a portion of the shell that is pointing towards the core (i.e., a "down" dipole moment) may decrease the conductance of the core, while a polarization state in the portion of the shell that is pointing away from the shell (i.e., an "up" dipole moment) will increase the conductance of the core. Additionally, the conductance of the core may be determined without changing the polarization state of the portion of the shell, e.g., by applying a voltage to the portion of the shell that is negative with respect to the voltage with which the polarization is written but smaller in value. One or more electrodes may be applied to the one or more portions of the shell in order to apply such voltages. Thus, by determining the conductance of the core proximate to each portion of the shell, the polarization state of that portion of the shell can be individually determined. For instance, higher conductance (e.g., with respect to the nanoscale wire before a reading voltage is applied) may indicate a lack of polarization in that portion of the shell (since a depolarized shell portion is typically not substantially altered by further depolarization), while a lower conductance may indicate polarization in that portion of the shell. Thus, the nanoscale wire may be treated as a transistor or a switch in some cases, where the core acts as a source and a drain, and each of the shell portions acts as a gate. By applying a reading voltage to each portion of the shell of a nanoscale wire in turn, the state of each portion of the nanoscale wire encoding data can be determined.

It should be understood that the invention is not limited only to barium titanate, but also includes other materials, such as ferroelectric oxide materials and/or other

electrically-polarizable materials or functional oxide materials. For example, in one aspect, the invention includes a material able to retain its polarization state in the absence of an external electric field.

As used herein, a "functional oxide" material is a material, comprising an oxide, forming a coating or a shell on at least a portion of a nanoscale wire. A functional oxide typically will functionally affect the nanowire with which it is associated, either by affecting an electronic and/or emissive and/or other property of the nanowire, or by serving as a platform at which to attach molecules materials that affect the nanowire or its function, or the like. Examples of functional oxide materials include, but are not limited to, a high-K dielectric material, a ferroelectric oxide material, a ferromagnetic oxide material, or the like, e.g. as described herein. Combinations of these and/or other materials are also contemplated in certain embodiments of the invention. In some cases, the functional oxide material may be deposited on a nanoscale wire using techniques such as atomic layer deposition or other techniques described herein.

As used herein, a "ferroelectric oxide material" is a material that can be reversibly and stably polarized by an external stimulus, for example, an electric field and/or mechanical stress, such that the material retains its polarization state even when the external stimulus is removed. (As is understood by those of ordinary skill in the art, it should also be noted that a "ferroelectric oxide" material, despite its name, is not restricted to iron-containing materials and/or materials containing oxygen.) Typically, the ferroelectric oxide material has two states, which may be referred to, variously, as a "polarized" state and a "depolarized" state (or an "oppositely polarized" state), an "up" electric dipole moment and a "down" electric dipole moment, a relatively high conductivity state and a relatively low conductivity state; a first state having a dipole moment and a second state not having a dipole moment, etc. It should be understood, in the descriptions herein, references to two states of a ferroelectric oxide material, such as a "polarized" and a "depolarized" state, are by way of example only, and that in that in other embodiments, the states of a ferroelectric oxide material may be referred to as an "up" electric dipole moment and a "down" electric dipole moment, a relatively high conductivity state and a relatively low conductivity state, etc. Non-limiting examples of ferroelectric oxide material include barium titanate ($BaTiO_3$), lead titanate ($PbTiO_3$), lead zirconium titanate ($Pb(Zr_{1-x}Ti_x)O_3$), strontium bismuth tantalate ($SrBi_2Ta_2O_6$), bismuth

lanthanum titanate ($Bi(La_xTi_{1-x})_4O_{12}$), strontium barium titanate ($Ba_xSr_{1-x}TiO_3$), germanium telluride (GeTe), or the like.

In one set of embodiments, the ferroelectric oxide material includes a material having a perovskite crystal structure, or an ilmenite crystal structure. Such crystal structures may have two or more one stable atomic states, for example, a first stable state where the atoms within the unit cell of the crystal structure are in a first position, and a second stable state where the atoms within the unit cell of the crystal structure are in a second position that is different from the first position. The perovskite crystal structure can thus be an electrically polarizable material that can be polarized in the first state or in the second state using different applied electric fields. Those of ordinary skill in the art will be able to identify materials having perovskite or ilmenite crystal structures. Examples of atoms which may be present within certain perovskite materials include, but are not limited to, barium, zirconium, titanium, lead, germanium, strontium, etc., as well as certain oxides thereof. In certain cases, the ferroelectric oxide material may comprise more than one type of unit cell. For example, the ferroelectric oxide material may comprise barium titanate and lead titanate, barium titanate and lead zirconium titanate, lead titanate and lead zirconium titanate, etc.

As used herein, a material or region that is "electrically polarizable" is a material whose polarization state may be changed upon the application of an electric field. In some embodiments, of the invention, the material or region that is electrically polarizable may be able to retain its polarization state when the electric field is removed, for example, in embodiments where the electrically-polarizable region comprises a ferroelectric oxide material and/or a functional oxide material. Thus, for example, a first electric field applied to a ferroelectric oxide material may cause the material (or at least a portion thereof) to enter a "polarized" state, and a second electric field may cause the material (or at least a portion thereof) to enter a "depolarized" or an "oppositely polarized" state. In some cases, the first electric field and the second electric field may have opposite signs (i.e., positive and negative electric fields). The electric field applied to the material or region may have an intensity and/or a duration at least sufficient to change the polarization state of the material or region. As discussed in more detail below, in some cases, the electrically-polarizable region may include two or more portions that can be independently polarized, i.e., a first portion of the electrically-

polarizable region can be polarized or depolarized without substantially altering the state of polarization of a second portion of the electrically-polarizable region, a first portion of the electrically-polarizable region in which the conductivity can be enhanced without substantially altering the conductivity of a second portion of the electrically-polarizable region, etc.

It should also be understood that the invention is not limited to nanoscale wires having a core and a shell, but also includes other arrangements of nanoscale wires and other nanostructures as well. For example, in one embodiment, a nanostructure may comprise a first layer or region that is electrically-polarizable, and a second layer or region that is semiconductive or conductive, e.g., as is illustrated in Fig. 6A with a semiconductive or conductive region 71 and an electrically-polarizable region 72. As another non-limiting example, the nanostructure may comprise two electrically-polarizable regions sandwiching a semiconductive or conductive region. Thus, in the descriptions below, it should be understood that references to nanoscale wires are by way of convenience only, and that other nanostructures may also be used in certain cases.

One set of embodiments provides a nanoscale wire having a first region comprising a ferroelectric oxide material (e.g., as previously discussed), and a second region, which may be free of a ferroelectric oxide material. For example, the second region may comprise a semiconductor such as silicon, a conductor, a high-K dielectric material, a metal, etc. Another set of embodiments provides a nanoscale wire having a first region that comprise a perovskite crystal structure and/or an ilmenite crystal structure, and a second region that is free of a perovskite crystal structure and/or an ilmenite crystal structure. Yet another set of embodiments provides a nanoscale wire having a first region that is electrically-polarizable, and a second region that is not electrically-polarizable. Still another set of embodiments provides a nanoscale wire having a first region that has a dielectric constant of at least about 15, and a second region having a dielectric constant less than the first region. Yet another set of embodiments of the invention provides a nanoscale wire having a first region comprising a functional oxide material, and a second region which may be free of a functional oxide material. Combinations of these embodiments are also possible in some cases. More than two regions within a nanoscale wire are also possible (for example, the nanoscale wire may have two, three, four, five, or more such regions), and these regions may have

unique compositions and/or some of these regions may comprise the same compositions, e.g., as is shown in Figs. 4B and 4C.

The regions may be positioned in any arrangement with respect to each other, for example, radially (e.g., as in a core/shell structure, as shells of a core/shell structure, etc.) or longitudinally (e.g., the regions may be adjacently positioned along a longitudinal axis of the nanoscale wire). Combinations of these arrangements are also possible. For example, a nanoscale wire may have a first region and a second region adjacently positioned to the first region along a longitudinal axis of the nanoscale wire, surrounded by at least one shell; the nanoscale wire may have two, three, or more shells at least partially surrounding a core, etc. Each region may have any shape or dimension. For instance, a region may have a smallest dimension of less than 1 micrometer, less than 100 nm, less than 10 nm, or less than 1 nm. In some cases, one or more regions may comprise a single monolayer of atoms. In certain arrangements, the region may be less than a single monolayer thick (for example, if some of the atoms within the monolayer are absent). The regions of the nanoscale wire may be distinct from each other with minimal cross-contamination (for example, the junction between two differing regions may be "atomically-abrupt," where there is a sharp transition at the atomic scale between two adjacent regions that differ in composition), or the composition of the nanoscale wire may vary gradually from one region to the next. As an example, an "overlap region" between adjacent regions may be a few nanometers wide, for example, less than about 10 nm, less than about 20 nm, less than about 40 nm, less than about 50 nm, less than about 100 nm, or less than about 500 nm. In some cases, an additional, separation region may be added to the nanoscale wire to separate these regions. For instance, the separation region may prevent or at least reduce atomic diffusion between other regions of the nanoscale wire.

A nanoscale wire may have two, three, or more shells at least partially surrounding a core (e.g., a "core/shell arrangement"), according to some embodiments of the invention. For example, in Fig. 4B, nanoscale wire 5 comprises core 10 and shells 20 and 30 (concentrically arranged), while in Fig. 4C, nanoscale wire 5 comprises core 10 and shells 20, 30, and 40 (concentrically arranged). The shells may be radially (i.e., concentrically) positioned around at least a portion of the core, and/or longitudinally positioned relative to each other (e.g., contacting each other, defining a change in

composition or concentration of a unitary shell structure longitudinally, separated from each other by, e.g., air, an insulator, a fluid, or an auxiliary, non-nanowire component, etc.). The shell portions can be positioned directly on the core, or can be separated from the core by one or more intermediate shells portions that can themselves be consistent in composition longitudinally, or varying in composition longitudinally. The shells do not necessarily have to be concentrically arranged; for example, one or more of the shells may be positioned off-center with respect to the core.

One set of embodiments of the invention additionally includes a high-K dielectric material, for example, positioned as a shell or other region of a nanoscale wire or other nanostructure. The high-K dielectric material may be positioned anywhere within the nanoscale wire. As used herein, a "high-K dielectric material" is a material that is generally a poor conductor of electricity, but is a relatively efficient supporter of an electric field, i.e., the material permits an electric field to be transmitted therethrough, but does not readily permit an electric current to pass. Such properties may be determined, for instance, by determining the dielectric constant ("K") of the material, using techniques known to those of ordinary skill in the art. A high-K dielectric material may have a relatively high dielectric constant, for example, a dielectric constant of at least about 10, and in some cases, the dielectric constant may be at least about 15, at least about 20, at least about 25, at least about 30, at least about 40, or at least about 50. Non-limiting examples of materials having relatively high dielectric constants include certain ceramic materials, mica, glass, or certain polymers. In some embodiments, the high-K dielectric material may include materials that comprise compounds of zirconium, hafnium, aluminum, etc. having relatively high dielectric constants. In one embodiment, the high-K dielectric material includes one or more oxides (i.e., inorganic materials comprising one or more oxygen atoms). Those of ordinary skill in the art will know of oxides having suitable dielectric constants. Non-limiting examples include metal oxides, for example, comprising zirconium or hafnium; specific examples include ZrO_2, $ZrSiO_4$, HfO_2, $HfSiO_4$, Al_2O_3, or the like. In some cases, more than one material having a high dielectric constant may be used.

In some embodiments, the high-K dielectric material may be positioned between a semiconductive or conductive region of a nanoscale wire, and an electrically polarizable region in a nanoscale wire. The high-K dielectric material may be chosen to

have a dielectric constant, according to some embodiments, such that the material is able to enhance the ability of the electrically polarizable region to retain its polarization state, for example, by preventing or at least limiting current flow between the semiconductive or conductive region and the electrically polarizable region. In some cases, e.g., if the nanoscale wire has a core/shell arrangement where the semiconductive or conductive region is the core and the electrically polarizable region is a shell of the nanoscale wire, the high-K dielectric material may be positioned as another shell of the nanoscale wire, for instance, positioned between at least a portion of the electrically polarizable shell and at least a portion of the core of the nanoscale wire. As an example, in Fig. 4B, nanoscale wire 5 may comprise a semiconductive or conductive core 5, an inner shell 30 comprising a high-K dielectric material, and an outer shell 20 comprising an electrically polarizable material.

The high-K dielectric material may be positioned directly adjacent to the semiconductive or conductive region, and/or to the electrically polarizable region, or indirectly positioned such that an electric field created between the semiconductive or conductive region and the electrically polarizable region substantially contacts at least a portion of the high-K dielectric material (e.g., to an extent that can be measured). For example, another region of material (for example, comprising a metal, as discussed below) may be positioned between the high-K dielectric material and the electrically polarizable region.

As other examples, in some embodiments, the high-K dielectric material may be positioned, directly or indirectly, between two or more regions of a nanoscale wire, for example, between two or more regions as previously described. For instance, the high-K dielectric material may be positioned between a first region comprising a ferroelectric oxide material and a second region free of a ferroelectric oxide material, between a first region comprising a perovskite crystal structure and/or an ilmenite crystal structure and a second region free of a perovskite crystal structure and/or an ilmenite crystal structure, between a first region having a dielectric constant of at least about 15 and a second region having a dielectric constant less than the first region, between a first region comprising a functional oxide material and a second region free of a functional oxide material, etc.

Another set of embodiments of the invention additionally includes a separation region separating two or more other regions within a nanoscale wire or other nanostructure, for example, a semiconductive or conductive region, and/or an electrically polarizable region, or any of the other regions described above. The separation region may prevent (or at least reduce) atomic diffusion to other regions of the nanoscale wire. In some embodiments, the separation region can be defined by a material having an intraatomic diffusion coefficient that is less than the regions adjacent the separation region. In another embodiment, the separation region may include a metal (e.g., a noble metal, such as gold or platinum), or an oxide (e.g., SiO_2). In yet another embodiment, the separation region includes, or is defined by, a high-K dielectric material. Thus, with reference to Fig. 4B, a nanoscale wire 5 may comprise a semiconductive or conductive core 5, an outer shell 20 comprising an electrically polarizable material, and a separation region 30 separating the semiconductive or conductive core and the electrically polarizable material.

In still another set of embodiments; the nanoscale wire or other nanostructure includes a region comprising a metal, for example, separating two or more other regions within a nanoscale wire, for instance, a semiconductive or conductive region, and/or an electrically polarizable region, or any of the other regions described above. The region comprising the metal may allow a better connection to be made between regions of the nanoscale wire, for example, due to a reduction in strain due to differences in atomic spacing between the different regions. In some cases, the metal region may also be used to prevent or at least reduce atomic diffusion to other regions of the nanoscale wire. Examples include, but are not limited to, noble metals such as gold, platinum, palladium, rhodium, silver, or iridium.

It should be understood that any combination of the regions described above are contemplated in certain embodiments of the invention. Thus, for example, a nanoscale wire or another nanostructure may comprise a semiconductive or conductive region, a high-K dielectric material, a region comprising a metal, and an electrically polarizable region, and in some cases, these regions may be distributed in a core/shell arrangement. Thus, as is illustrated in Fig. 4C as an example, a nanoscale wire 5 may comprise a semiconductive or conductive core 5, a first shell 30 surrounding at least a portion of the core comprising a high-K dielectric material, a second shell 40 surrounding at least a

portion of the first shell comprising a metal, and an outer shell 20 surrounding at least a portion of the second shell comprising an electrically polarizable material. In some cases, the shells may be concentrically arranged around the core.

In one set of embodiments, the nanoscale wire or other nanostructure comprises an electrically-polarizable region that includes two or more portions that can be independently polarized. For instance, a first portion of an electrically-polarizable region can be polarized or depolarized without substantially altering the polarization state of an adjacent portion of the nanoscale wire. Thus, upon electrically polarizing or depolarizing the first portion of the electrically-polarizable region, the polarization state of the second portion of the electrically-polarizable region is not substantially altered (e.g., the second portion is not simultaneously polarized or depolarized), and when read (as discussed below), results in the same data as prior to polarization or depolarization of the first portion.

In one embodiment, the portions of the electrically-polarizable region that can be independently polarized or depolarized are separated by a distance (center-to-center) of at least 3 unit cells, and in some cases, the portions may be separated by a distance of at least 4 unit cells, at least 5 unit cells, at least 7 unit cells, at least 10 unit cells, at least 15 unit cells, at least 20 unit cells, at least 25 unit cells, at least 50 unit cells, etc. As used herein, a "unit cell" is the simplest repeating unit in the crystal structure of the electrically-polarizable region. Those of ordinary skill in the art will know of suitable techniques for determining the unit cell size of a material. As a specific example, if the electrically-polarizable region comprises a $BaTiO_3$ perovskite crystal structure, the unit cell size may be about 0.4 nm.

In another embodiment, the portions of the electrically-polarizable region that can be independently polarized or depolarized are defined by one or more electrodes, each independently positioned in contact or proximate to the electrically-polarizable region (i.e., at a distance such that, when an electric field of suitable intensity and duration is applied using the electrode, the portion of the electrically-polarizable region proximate the electrode is polarized or depolarized without adjacent regions of the nanoscale wire being substantially altered). In some cases, at least one electrode is in contact or is proximate to the electrically-polarizable region, and in some cases, at least 2, 3, 5, 10, 20, 50, 75, or 100 electrodes each are in contact and/or are proximate to the electrically-

polarizable region, for example, in contact or proximate to different portions of the electrically-polarizable region. In certain, but not all, instances, for example, due to practical considerations, no more than 100, 50, 20, or 10 electrodes each are in contact or are proximate to the electrically-polarizable region. As further discussed below, in some cases, a nanoscale wire may be used to encode more than one bit of data, and in certain embodiments of the invention, each electrode may be used to encode and/or read bits of data in the nanoscale wire.

In some embodiments, the electrodes may be positioned such that they are separated by a distance of at least a 3 unit-cell spacing of the electrically-polarizable region. In other embodiments, however, the electrodes may be positioned such that they are separated by greater distances. For example, in some cases, the electrodes are positioned such that they are separated by a distance of at least 4 unit cells, at least 5 unit cells, at least 7 unit cells, at least 10 unit cells, at least 15 unit cells, at least 20 unit cells, at least 25 unit cells, at least 50 unit cells, etc. with respect to the electrically-polarizable region. In other cases, the electrodes may be separated by a distance of at least about 1 nm, at least about 2 nm, at least about 3 nm, at least about 5 nm, at least about 10 nm, at least about 15 nm, at least about 20 nm, at least about 25 nm, at least about 30 nm, at least about 40 nm, at least about 50 nm, at least about 75 nm, at least about 100 nm, at least about 150 nm, at least about 200 nm, at least about 250 nm, at least about 300 nm, at least about 500 nm, or at least about 1 micron.

In one embodiment, as schematically illustrated in Fig. 5, the spacing between the electrodes is determined by fabricating core-shell nanoscale wires (Fig. 5A), aligning the nanoscale wires and spacing them to a certain pitch and/or such that the nanoscale wires are in contact (for example, using Langmuir-Blodgett techniques such as those disclosed in Serial No. 60/524,301, entitled "Nanoscale Arrays and Related Devices," filed November 20, 2003, incorporated herein by reference) (Fig. 5B), then etching away at least a portion of the shells of the nanoscale wires using suitable etching techniques, such that the cores define the electrodes (Fig. 5C). The electrode array may be positioned in contact or at least proximate to the nanoscale wire using transfer techniques known to those of ordinary skill in the art, for example, using stamping or imprinting techniques as disclosed in Serial No. 60/524,301, entitled "Nanoscale Arrays and Related Devices," filed November 20, 2003, or Serial No. 10/995,075, entitled "Nanoscale Array and

Related Devices," filed November 22, 2004, each incorporated herein by reference, and the electrode array may be positioned at any suitable point during the fabrication process, for instance, before or after the shells have been etched. As used herein, the "pitch" of an array of nanoscale wires is the spacing between the centers of adjacent nanoscale wires. The pitch may be, for example, less than about 500 nm, less than about 200 nm, less than about 100 nm, less than about 50 nm, or less than about 20 nm in some cases. In other embodiments, the pitch of the nanoscale wires may be at least about 100 nm, at least about 200 nm, at least about 300 nm, at least about 400 nm, at least about 500 nm, at least about 600 nm, at least about 750 nm, at least about 1 micron, at least about 2 microns, at least about 3 microns, at least about 5 microns, at least about 10 microns, at least about 15 microns, at least about 20 microns, or at least about 25 microns or greater. In certain embodiments, the aligned nanoscopic wires are arranged such that they are in contact with each other; in other embodiments, however, the aligned nanoscopic wires may be at a pitch such that they are not in substantial physical contact.

The electrodes can be fabricated from any material able to transmit a voltage to the nanoscale wire, e.g., to the electrically-polarizable region. The electrodes may each independently be fabricated from the same or different materials. For example, the electrodes can comprise a metal (e.g., nickel, copper, a noble metal, such as gold or platinum, etc.), or a semiconductor material (e.g., silicon, gallium, germanium, etc.). In one embodiment, one or more or electrodes may comprise another nanoscale wire.

The electrodes can be positioned in contact or at least proximate to the electrically-polarizable region of the nanoscale wire using any suitable technique known to those of ordinary skill in the art, for example, using electron beam lithography or photolithography techniques, for instance, followed by metal deposition (e.g. thermal evaporation, electron beam evaporation, etc. of a metal such as nickel, titanium, noble metals such as palladium, etc.). Typically, the electrodes are immobilized with respect to the nanoscale wire (i.e., the electrode does not move with respect to the nanoscale wire). Thus, the immobilized electrode can be used to define, in some embodiments, a portion of the electrically-polarizable region of the nanoscale wire that can be used to encode a bit of data.

It should be noted, however, that electrodes are not necessarily required in all embodiments. For instance, in some cases, an electric field may be applied to the

nanoscale using a device external to the nanoscale wire. For example, a probe such as an atomic force microscope ("AFM") probe may be positioned proximate to or in contact with the nanoscale wire, and used to apply an electric field to the portion of the electrically-polarizable region of the nanoscale wire.

In some aspects of the invention, one or more bits of data may be encoded into a nanoscale wire or other nanostructure of the invention, for instance, by using a nanoscale wire comprising an electrically-polarizable region that includes two or more portions that can be independently polarized, as described above. For example, a first polarization state can be assigned "0" (for example, a depolarized state, a relatively high conductivity state, etc.) and a second polarization state can be assigned "1" (for example, a polarized state, a relatively low conductivity state, etc.). It should be noted that, as used herein, the term "bit" or "bits" is used relative to data and typically has two states, often referred to as "0" and "1"; while the term "bit" or "bits," as used to measure information content in an information theory sense (for example, when a computer file is mathematically "compressed" to reduce the file size, such that each "bit" is thereby used to encode multiple pieces of information) is not used herein.

Thus, a nanoscale wire of the invention may include an electrically-polarizable region comprising any number of portions that can each be independently polarized or depolarized, and such a nanoscale wire may be used to encode a similar number of bits of data. For example, at least 1, 2, 3, 5, 10, 20, 50, 75, or 100 bits of data may be encoded within a nanoscale wire of the invention. The actual number of a nanoscale wire may depend on factors such as the size or length of the nanoscale wire, the number of electrodes positioned adjacent or proximate the nanoscale wire, etc. In certain instances, for example, due to practical considerations, no more than 100, 50, 20, or 10 bits of data may be encoded within the nanoscale wire.

As previously discussed, in certain embodiments of the invention, one or more electrodes positioned in contact or at least proximate to the electrically-polarizable region may be used to define one or more portions of the electrically-polarizable region, each independently capable of encoding a bit of data. The electrodes may be used to encode (write) and/or read bits of data to/from the nanoscale wire.

In one set of embodiments, a portion of an electrically-polarizable region may be polarized (e.g., to encode a bit of data, for example, a "1") by applying an electric field to

that portion that has an intensity and/or a duration at least sufficient to cause that portion to be polarized (e.g., using a "writing" voltage to create the electric field). Thus, according to this embodiment, if the portion was previously depolarized, the region is now polarized; if the portion was previously polarized, the region remains polarized. The electric field may be applied to the portion of an electrically-polarizable region using any suitable technique. For example, the electric field may be created using the nanoscale wire (for instance, by applying a current to a semiconductive or conductive region of a nanoscale wire), or the electric field may be externally applied to the nanoscale wire, for example, using an electrode, an external probe, etc. As a specific, non-limiting example, in Fig. 6A, a nanoscale wire or other nanostructure 75 comprises a semiconductive or conductive region 71 and an electrically-polarizable region 72, and electrode 76 is positioned proximate the electrically-polarizable region of the nanoscale wire; an electric field may be created across the electrically-polarizable region by creating a potential difference between electrode 76 and semiconductive or conductive region 71, for instance, by applying a voltage to electrode 76 while applying a different voltage to region 71 (e.g., a greater or lesser voltage, a voltage having the opposite sign, no voltage, etc.).

Relatively low "writing" voltages may be used in some cases, due to the nanoscopic nature of the wire. For example, in one set of embodiments, voltages having a magnitude (i.e., ignoring sign) of less than about 5 V, less than about 4.5 V, less than about 4 V, less than about 3.5 V, less than about 3 V, less than about 2.5 V, less than about 2 V, less than about 1.8 V, less than about 1.6 V, less than 1.4 V, less than about 1.2 V, less than about 1 V, less than about 0.8 V, or less than about 0.5 V may be used to alter the polarization state of the portion of an electrically-polarizable region. In some cases, the writing voltage may also be greater than a certain value, for example, greater than 2 V, greater than 3 V, greater than 4 V, etc. As non-limiting examples, the writing voltage may be between about 3 V and about 5 V, between about 4 V and about 5 V, etc. The voltage applied may be sufficient to alter the polarization state of the electrically-polarizable region (for example, from a depolarized state to a polarized state).

In some embodiments, the magnitude voltage required to polarize the portion of the electrically-polarizable region may be greater than (or less than) the magnitude of the voltage required to depolarize the portion of the electrically polarizable region, i.e., the

magnitudes of the polarization and depolarization voltages are not equal. As an example, in one embodiment, the voltage that may be required to polarize ("writing") the portion of the electrically polarizable region may be between +4 V and +5 V, while the voltage required to depolarize ("erase") the portion of the electrically polarizable region bay be between -3 V and -4 V.

In one embodiment, an electric field is created by creating a potential difference between an electrode or other probe positioned in contact or at least proximate to the portion of the electrically-polarizable region, and a semiconductive or conductive region of the nanoscale wire. For example, a voltage may be applied to the electrode while the semiconductive or conductive region is grounded or a voltage of the opposite sign is applied to the semiconductive or conductive region, or a relatively larger voltage may be applied to the electrode while a relatively smaller voltage is applied to the semiconductive or conductive region or the region is grounded. Similarly, the portion of the electrically-polarizable region may be depolarized (e.g., to encode a bit of data, for example, a "0") by applying an electric field to that portion that has an intensity and/or a duration at least sufficient to cause that portion to be depolarized, for example, by applying an electric field, having an opposite sign to the polarizing electric field, to that portion of the electrically-polarizable region using techniques similar to those described above. As before, if the portion was previously polarized, the region is now depolarized; if the portion was previously depolarized, the region remains depolarized (or oppositely polarized).

If the nanoscale wire comprises more than one portion that can be electrically polarized, the various portions may be independently polarized or depolarized. For example, in one embodiment, a first electric field may be applied to a first portion, and a second electric field (which may be the same or different than the first electric field, or which may be absent, i.e., having zero intensity) may be applied to a second portion of the nanoscale wire. As a specific example, with reference to Fig. 6B, nanoscale wire 5 comprises a semiconductive or conductive core 10 and an electrically-polarized shell 20; a first electrode 60 and a second electrode 65 are positioned proximate the nanoscale wire, defining at least two portions 11, 12 that can be used to independently encode bits of data. Portion 11 may be polarized without substantially altering the polarization state of portion 12 by applying an electric field 50 to only portion 11, for instance, by

applying a positive voltage to electrode 60 while simultaneously grounding or applying a negative voltage to core 10 and electrode 65, by applying a voltage to electrode 60 while grounding or applying a negative voltage to core 11 and applying a voltage slightly less than the voltage of the core to electrode 11 (thereby creating an electric field proximate to portion 12 that tends to negate any "spill-over" effects on portion 12 caused by electric field 50), by applying a greater voltage to electrode 60, relative to core 10 and/or electrode 65 (for example, in devices where a "floating" voltage used), or the like.

The polarization state of the portion of an electrically-polarizable region may be determined using any suitable technique, including those previously described. For example, in one set of embodiments, the polarization state may be determined by applying a voltage (i.e., a "reading" voltage) to the portion of the electrically-polarizable region while simultaneously measuring the conductance of a semiconductive or conductive region of the nanoscale wire positioned adjacent or proximate the electrically-polarizable region (i.e., positioned such that the polarization state of the portion of the electrically-polarizable region alters the conductance of the semiconductive or conductive region), for example, if the electrically-polarizable region comprises a ferroelectric oxide material or a functional oxide material. In some cases, the voltage may be applied to the portion of the electrically-polarizable region using an electrode positioned in contact or at least proximate to the portion of the electrically-polarizable region. In certain instances, the electrode or other probe may also be the electrode used to polarize ("write" or "encode") the electrically-polarizable region.

Typically, the voltage applied to the portion of the electrically-polarizable region does not have an intensity and/or a duration sufficient to alter the polarization state of the portion of the electrically-polarizable region. For example, if the electrically-polarizable semiconductive region comprises p-type doped silicon, and polarization is "written" to at least one portion of the electrically-polarizable region, then a positive voltage applied to a polarized portion may decrease the conductance of the semiconductive or conductive region, relative to the absence of the applied voltage, while a negative voltage applied to the polarized portion may increase the conductance of the semiconductive or conductive region, relative to the absence of the applied voltage. Thus, as a specific, non-limiting example, with reference to Fig. 6A, the polarization state of electrically-polarizable region 72 can be determined by applying a voltage (insufficient to alter the polarization

state of region 72), and measuring the resulting change in conductance of semiconductive or conductive region 71, for example, by applying a potential drop from a first end 77 to a second end 78 of region 71, and measuring the resulting current.

In certain instances, relatively low "reading" voltages may be used to determine the polarization state, due to the nanoscopic nature of the wire. For example, in one set of embodiments, voltages having a magnitude of less than about 5 V, less than about 3 V, less than about 2.5 V, less than about 2 V, less than about 1.8 V, less than about 1.6 V, less than 1.4 V, less than about 1.2 V, less than about 1 V, less than about 0.8 V, or less than about 0.5 V may be used to determine the polarization state of the portion of an electrically-polarizable region. Additionally, in other embodiments, the read/write voltage ratio may also be kept relatively low. For example, the ratio between the reading voltage and the writing voltage may be less than about 1:10, less than about 1:5, less than about 1:3, less than about 1:2.5, less than about 1:2, less than about 1:1.8, less than about 1:1.6, less than about 1:1.5, less than about 1:1.4, less than about 1:1.3, less than about 1:1.2, or less than about 1:1.1. In some embodiments, different ratios of read/write voltages may be used for different portions of the nanoscale wire.

If the nanoscale wire comprises more than one portion that can be electrically-polarized, each portion may be independently determined (and/or combinations of portions may be determined, in some cases, for example, as discussed below in Example 1). For example, in one embodiment, a first electric field may be applied to a first portion, and a second electric field (which may be the same or different than the first electric field, or which may be absent, i.e., having zero intensity) may be applied to a second portion of the nanoscale wire. As a specific example, with reference to Fig. 6B, the polarization state of portion 11 may be determined by determining the conductance of core 11 when a voltage (i.e., a reading voltage) is applied to electrode 60 (and no voltage is applied to electrode 65), relative to the conductance of core 11 when no voltages are applied to electrodes 60 or 65. The conductance of core 11 may be determined using any suitable technique for measuring technique known to those of ordinary skill in the art. For instance, a potential drop may be created from a first end 15 of core 11 to a second end 16 of core 11, and the resulting current may then be measured.

It should also be noted that certain aspects of the invention can be used as a transistor or a switch. For instance, in one set of embodiments, an electrically-

polarizable region of a nanoscale wire or other nanostructure may be used as a "gate," while a semiconductive or conductive region of the nanoscale wire positioned in contact or at least proximate the electrically-polarizable region may be used as a "source" and a "drain" of the transistor or switch. Thus, as a specific example, Fig. 6A can be used to illustrate a switch, where electrically-polarizable region 72 acts as a control terminal or a "gate," while a first end 77 of semiconductive or conductive region 71 acts as a first terminal or a "source," and a second end 78 of region 71 acts as a second terminal or a "drain." A potential, applied to electrode 76, may be used to alter the polarization state of electrically-polarizable region 72, which may thereby alter the conductivity between the first and second terminals, or between the source and the drain.

Additionally, in some cases, the nanoscale wire transistor may have more than one control terminal or "gate." For example, in some embodiments, each electrode positioned in contact or proximate to a portion of an electrically-polarizable region of a nanoscale wire may define a terminal or "gate" region of that portion of the electrically-polarizable region. As a non-limiting example, with reference to Fig. 6B, nanoscale wire 5 may act as a switch, having a source (first terminal 15), a drain (second terminal16), a first gate region (first portion 11), and a second gate region (second portion 12). An electric potential may be applied to either (or both) of control terminals 60 and 65, which each may be used to alter the polarization state of respective portions 11 and 12, each of which may thereby alter the conductivity between the source (first terminal 15) and the drain (second terminal 16).

Thus, one aspect of the invention provides devices comprising any of the nanoscale wire or nanostructure embodiments described herein, including memory devices and/or devices comprising transistors, switches, or the like. Some devices may include one, or more than one, of the nanoscale wire embodiments described herein.

In one set of embodiments of the present invention, a nonvolatile memory is provided. A nanoscale wire of the invention may be used to encode one, or more than one, bit of data, and such nanoscale wires can retain the data even in the absence of power. In some cases, an array of nanoscale wires may be used as nonvolatile memory. In certain embodiments, a relatively high density of memory elements can be achieved. For example, in some cases, the device may comprise an array of memory elements, each having an area of less than about 100 nm^2/bit, less than about 75 nm^2/bit, less than about

50 nm^2/bit, less than about 30 nm^2/bit, less than about 25 nm^2/bit, less than about 20 nm^2/bit, less than about 15 nm^2/bit, less than about 10 nm^2/bit, less than about 8 nm^2/bit, less than about 6 nm^2/bit, or less than about 4 nm^2/bit.

In one embodiment, an array of memory elements can be assembled using one or more nanoscale wires of the invention, crossed with one or more electrodes (e.g., as described herein). The electrodes may contact single nanoscale wires, or in some cases, the electrodes may contact more than one nanoscale wire, for example, as is illustrated in Fig. 8A. By systematically controlling the potential of each of the nanoscale wires and each of the electrodes, specific voltages can be made to appear at any desired location or locations within the array, which can then be used to read and/or write data to those locations, using techniques similar to those previously described. Thus, each intersection between a nanoscale and an electrode may define a portion of an electrically-polarized region that can encode a bit of data. Those of ordinary skill in the art, with the benefit of the present disclosure, will be able to identify suitable systems and methods for using an array comprising rows and columns for storing and accessing bits of data at the intersections of the rows and columns.

One non-limiting example of a memory array is as follows. With reference to Fig. 8A, memory array 100 comprise a series of nanoscale wires 101, 102, 103, ... In this figure, each of nanoscale wires 101, 102, 103, ... has a core that is semiconductive or conductive, and a shell that is electrically polarizable. Of course, in other embodiments, other nanoscale wires are also possible, for instance, any of the nanoscale wires as previously described, and in some cases, each of the nanoscale wires may independently be the same or different. In Fig. 8A, each of nanoscale wires 101, 102, 103, ... is in contact (or at least proximate to) a series of electrodes 111, 112, 113, ... Electric fields may be created at any desired location or locations within the array by controlling the voltages applied to each of the nanoscale wires and each of the electrodes. Thus, for example, to create an electric field at the junction of nanoscale wire 101 and electrode 111, a voltage may be applied to nanoscale wire 101 while a different voltage (or no voltage) is applied to electrode 111, a voltage may be applied to electrode 111 while no voltage is applied to nanoscale wire 101, a voltage is applied using a probe external the array, etc.

In this example, data may be written to an intersection by causing the nanoscale wire and the electrode defining the electrode to have potentials such that their difference is at least sufficient to encode a desired polarization state, while simultaneously "floating" the other nanoscale wires and electrodes (e.g., at an intermediate voltage, or at the voltage applied to the nanoscale wire), such that the electric potentials appearing elsewhere are not able to alter the polarization at those respective locations. Now referring to the schematic diagram of Fig. 8B, in memory array 100, a writing voltage is applied to nanoscale wire 101, while electrode 111 is grounded (or is brought to another relatively low voltage). The remaining nanoscale wires 102, 103, ... and electrodes 112, 113, ... can be electrically isolated, held at the writing voltage, and/or are held at an intermediate voltage between the writing voltage and the ground. The voltage difference at intersection 121 defined by the intersection of nanoscale wire 101 and electrode 111 is sufficient to polarize (or depolarize) that portion of the electrically-polarizable shell of nanoscale wire 101, thereby encoding a desired polarization state (e.g., representing a "1" or a "0"), while the voltage differences (if any) created at the other intersections in array 100 (e.g., between the writing voltage and the floating voltage, or between the floating voltage and ground) are insufficient to substantially alter the polarization states at those intersections. By applying suitable voltages to the other nanoscale wires and/or electrodes, each intersection within memory array 100 can be individually addressed and polarized or depolarized as desired.

Reading data from the memory array, in this example, can be performed by creating a potential across one of the nanoscale wires while simultaneously "floating" the other nanoscale wires (i.e., such that the potential difference across those nanoscale wires is negligible, for example, at the reading voltage), and applying voltages to each of the electrodes in turn and measuring the resulting conductivity of the nanoscale wire with the potential. Referring now to Fig. 8C, the polarization state of intersections 121, 122, 123, ... are to be determined (for example, which may encode a series of bits, a byte, a nybble, a word of data, etc. within the memory array). A voltage is applied to a first end of nanoscale wire 101 while the second end of nanoscale wire 101 is grounded. Simultaneously, nanoscale wires 102, 103, ... are "floated," i.e., the same (or nearly the same) potential is applied to either end of each of these wires, and in some cases, at a potential equal or substantially equal to the reading voltage. The reading voltage is

applied to electrode 111 while no voltage is applied to electrodes 112, 113, ..., and the conductivity of the wire is determined and compared to the conductivity of the wire where no voltage is applied to any of the electrodes. As previously discussed, differences in polarization state of intersection 121 may lead to different conductivities, thus indicating the polarization state of intersection 121. Next, to determine the polarization state of intersection 122, a reading voltage is applied to electrode 112 while no voltage is applied to electrodes 111, 113, ...etc, using similar techniques, and the conductivity of nanoscale wire 101 is again determined. By reporting this procedure, the polarization states of each of intersections 121, 122, 123, ... can be determined, according to this example. Those of ordinary skill in the art will know of other methods of reading and/or writing bits of data from an array of intersections defined by rows and columns, where each intersection can be used to encode a bit of data.

In some cases, due to the nanoscale size of the instant device, relatively high read/write operations can be achieved. For example, data may be read and/or written to the device at a speed of at least about 5 Mb/s, at least about 10 Mb/s, at least about 15 Mb/s, at least about 20 Mb/s, at least about 25 Mb/s, at least about 30 Mb/s, at least about 35 Mb/s, at least about 40 Mb/s, at least about 50 Mb/s, at least about 55 Mb/s, at least about 60 Mb/s, at least about 65 Mb/s, at least about 70 Mb/s, at least about 75 Mb/s, at least about 80 Mb/s, at least about 85 Mb/s, at least about 85 Mb/s, at least about 90 Mb/s, at least about 95 Mb/s, or at least about 100 Mb/s or more.

In still another set of embodiments, a nanoscale wire of the invention may be used as part of a ferroelectric random-access memory (FeRAM) component, for example, as part of a "smart" card, a radiofrequency identification (RFID) tag, or the like. For example, one or more nanoscale wires may be used in certain memory architectures. For example, the nanoscale wire may be used in a 1T1C architecture (one transistor "T"/one capacitor "C") (e.g., as shown in Fig. 7A), a 2T2C architecture (e.g., as shown in Fig. 7B), a 8T4C architecture (e.g., as shown in Fig. 7C), a chain architecture (e.g., as shown in Fig. 7D), a 6T4C architecture, or the like. Those of ordinary skill in the art will understand techniques for using memory architectures such as these; as an example, in a 1T1C architecture as is shown in Fig. 7A to encode a polarization state, voltage may be applied to bit line 80, while plate line 85 is grounded; a depolarization state may be encoded by applying voltage to plate line 85 while

grounding bit line 80; and the polarization state may be determined by applying a voltage to plate line 85 while floating bit line 80 and measuring word line 88.

In yet other embodiments, the invention includes devices such as field effect transistors (FETs), bipolar junction transistors (BJTs), tunnel diodes, modulation doped superlattices, complementary inverters, light emitting devices, light sensing devices, biological system imagers, biological and chemical detectors or sensors, thermal or temperature detectors, Josephine junctions, nanoscale light sources, photodetectors such as polarization-sensitive photodetectors, gates, inverters, AND, NAND, NOT, OR, TOR, and NOR gates, latches, flip-flops, registers, switches, clock circuitry, static or dynamic memory devices and arrays, state machines, gate arrays, and any other dynamic or sequential logic or other digital devices including programmable circuits that use any of the nanoscale wire embodiments described herein. Also included are analog devices and circuitry, including but not limited to, amplifiers, switches and other analog circuitry using active transistor devices or switch devices, as well as mixed signal devices and signal processing circuitry. In some embodiments, the nanoscale wires of the present invention may be manufactured during the device fabrication process. In other embodiments, the nanoscale wires of the present inventions may first be synthesized, then assembled in a device.

Another aspect of the invention provides for the fabrication of any of the embodiments described herein. For example, one set of embodiments provides a method of depositing a material on a nanoscale wire (or other nanostructure) to form a region that is electrically-polarizable. Another set of embodiments provides a method of depositing a ferroelectric oxide material on a nanoscale wire to form a region comprising the ferroelectric oxide material. Yet another set of embodiments provides a method of depositing a functional oxide material on a nanoscale wire to form a region comprising the functional oxide material. Still another set of embodiments provides a method of depositing a material comprising a perovskite crystal structure and/or an ilmenite crystal structure on a nanoscale wire. Yet another set of embodiments provides a method of depositing a material having a dielectric constant of at least about 15 on a nanoscale wire. Another set of embodiments provides a method of depositing a metal on a nanoscale wire. Combinations of these embodiments are also possible in some cases. For instance, in certain embodiments, one or more materials may be deposited on the

nanoscale wire to form one or more shells, each of which at least partially surrounding the nanoscale wire. In some instances, the nanoscale wire may be not immobilized, relative to a substrate, e.g., the nanoscale wire is not permanently attached to a substrate.

In certain cases, a material may be deposited using atomic layer deposition, using suitable precursor materials. Those of ordinary skill in the art will be able to determine suitable precursor materials, depending on the particular nanoscale wire to be synthesized. For example, water may be used as an oxygen source, zirconium chloride may be used as a zirconium source, barium bis(pentamethylcyclopentadienyl) may be used as a barium source, titanium tetraisopropoxide may be used as a titanium source, etc., to deposit a material on a nanoscale wire using atomic layer deposition. More than one source may be used, simultaneously or sequentially, in some cases. For example, to deposit $BaTiO_3$ on a nanoscale wire, barium bis(pentamethylcyclopentadienyl), and titanium tetraisopropoxidemay be supplied on an alternating basis during an atomic layer deposition process. In one embodiment, an atomic layer deposition reaction may be performed to deposit material on a substrate (which may be up to one atom in thickness in some cases) by providing the substrate (e.g., a nanoscale wire), applying a pulse of a reactant, followed by a purge. Optionally, additional reactants and/or purges may be applied. The thickness of the deposition layer may be controlled by the number and/or duration of the reactants and/or purge cycles. As one non-limiting example, with reference to Fig. 11, a silicon nanoscale wire 131 may be grown, for example, using chemical vapor deposition techniques (e.g., as shown in Fig. 11, silicon nanoscale wire 131 is grown from a catalyst particle 130 using chemical vapor deposition). To deposit ZrO_2 on the silicon nanoscale wire (for example, as a shell 133 at least partially surrounding the nanoscale wire 131, forming a core/shell arrangement, top and side views shown in Fig. 11), $ZrCl_4$ may be used as precursor for Zr, and H_2O may be used as precursor for O. It should be understood that, in this example, the deposition of ZrO_2 is not limited to the use of $ZrCl_4$ and H_2O, and other precursors may be used instead of and/or in conjunction with $ZrCl_4$ and H_2O. In this example, ZrO_2 may be deposited on the silicon nanoscale wire at any desirable thickness, for example, less than 5 nm, or 2 to 3 nm thick. To deposit $BaTiO_3$ (for example, on the ZrO_2 and/on a silicon nanoscale wire, for instance, as is shown in Fig. 11, where $BaTiO_3$ may be deposited as a shell 132 surrounding the ZrO_2 shell 133 and the silicon core 131), barium

bis(pentamethylcyclopentadienyl) ($Ba(C_5Me_5)_2$) may be used as a precursor for Ba, titanium tetraisopropoxide ($Ti(O\text{-}iPr)_4$) may be used as a precursor for Ti, and H_2O may be used as a precursor for O. As before, it should be understood that the deposition of $BaTiO_3$ is not limited to the use of these compounds, and other precursors may be used instead and/or in conjunction with these. In this example, $BaTiO_3$ may be deposited on the silicon nanoscale wire at any desirable thickness, for example, at a thickness of 10-30 nm.

Other techniques useful for fabricating nanoscale wires include, but are not limited to, vapor phase reactions (e.g., chemical vapor deposition ("CVD") techniques such as metal-catalyzed CVD techniques, catalytic chemical vapor deposition ("C-CVD") techniques, organometallic vapor phase deposition-MOCVD techniques, atomic layer deposition, chemical beam epitaxy, etc.), solution phase reactions (e.g., hydrothermal reactions, solvothermal reactions), physical deposition methods (e.g., thermal evaporation, electron-beam evaporation, laser ablation, molecular beam epitaxy), vapor-liquid-solid ("VLS") growth techniques, laser catalytic growth ("LCG") techniques, surface-controlled chemical reactions, or the like, for instance, as disclosed in Serial No. 10/196,337, entitled "Nanoscale Wires and Related Devices," filed July 16, 2002, published as Publication No. 2003/0089899 on May 15, 2003, incorporated herein by reference. As a non-limiting example, if a nanoscale wire having a core/shell arrangement is to be fabricated, the core may be fabricated using one of these techniques, and one or more shells may be at least partially coated on at least a portion of the core, for example, using CVD techniques, LCG techniques, atomic layer deposition, or the like.

Definitions

The following definitions will aid in the understanding of the invention. Certain devices of the invention may include wires or other components of scale commensurate with nanometer-scale wires, which includes nanotubes and nanowires. In some embodiments, however, the invention comprises articles that may be greater than nanometer size (e. g., micrometer-sized). As used herein, "nanoscopic-scale," "nanoscopic," "nanometer-scale," "nanoscale," the "nano-" prefix (for example, as in "nanostructured"), and the like generally refers to elements or articles having widths or

diameters of less than about 1 micrometer, and less than about 100 nm in some cases. In all embodiments, specified widths can be a smallest width (i.e. a width as specified where, at that location, the article can have a larger width in a different dimension), or a largest width (i.e. where, at that location, the article has a width that is no wider than as specified, but can have a length that is greater).

The term "plurality," as used herein, means two or more. A "set" of items may include one or more of such items.

The term "fluid" generally refers to a substance that tends to flow and to conform to the outline of its container. Typically, fluids are materials that are unable to withstand a static shear stress. When a shear stress is applied to a fluid, it experiences a continuing and permanent distortion. Typical fluids include liquids and gases, but may also include free-flowing solid particles, viscoelastic fluids, and the like.

As used herein, a "wire" generally refers to any material having a conductivity of or of similar magnitude to any semiconductor or any metal, and in some embodiments may be used to connect two electronic components such that they are in electronic communication with each other. For example, the terms "electrically conductive" or a "conductor" or an "electrical conductor" when used with reference to a "conducting" wire or a nanoscale wire, refers to the ability of that wire to pass charge. Typically, an electrically conductive nanoscale wire will have a resistivity comparable to that of metal or semiconductor materials, and in some cases, the electrically conductive nanoscale wire may have lower resistivities, for example, a resistivity lower than about 10^{-3} Ohm m, lower than about 10^{-4} Ohm m, or lower than about 10^{-6} Ohm m or 10^{-7} Ohm m.

A "nanoscopic wire" (also known herein as a "nanoscopic-scale wire" or "nanoscale wire") generally is a wire, that at any point along its length, has at least one cross-sectional dimension and, in some embodiments, two orthogonal cross-sectional dimensions less than 1 micron, less than about 500 nm, less than about 200 nm, less than about 150 nm, less than about 100 nm, less than about 70, less than about 50 nm, less than about 20 nm, less than about 10 nm, or less than about 5 nm. In other embodiments, the cross-sectional dimension can be less than 2 nm or 1 nm. In one set of embodiments, the nanoscale wire has at least one cross-sectional dimension ranging from 0.5 nm to 100 nm or 200 nm. In some cases, the nanoscale wire is electrically conductive. In some embodiments, the nanoscale wire is cylindrical. In other embodiments, however, the

nanoscale wire can be faceted, i.e., the nanoscale wire may have a polygonal cross-section. Where nanoscale wires are described having, for example, a core and a shell, the above dimensions generally relate to those of the core. The cross-section of a nanoscopic wire may be of any arbitrary shape, including, but not limited to, circular, square, rectangular, annular, polygonal, or elliptical, and may be a regular or an irregular shape. The nanoscale wire may be solid or hollow. Any nanoscale wire can be used in any of the embodiments described herein, including carbon nanotubes, molecular wires (i.e., wires formed of a single molecule), nanorods, nanowires, nanowhiskers, organic or inorganic conductive or semiconducting polymers, and the like, unless otherwise specified. Other conductive or semiconducting elements that may not be molecular wires, but are of various small nanoscopic-scale dimensions, can also be used in some instances, e.g. inorganic structures such as main group and metal atom-based wire-like silicon, transition metal-containing wires, gallium arsenide, gallium nitride, indium phosphide, germanium, cadmium selenide, etc. A wide variety of these and other nanoscale wires can be grown on and/or applied to surfaces in patterns useful for electronic devices in a manner similar to techniques described herein involving the specific nanoscale wires used as examples, without undue experimentation. The nanoscale wires, in some cases, may be formed having dimensions of at least about 1 micrometer, at least about 3 micrometers, at least about 5 micrometers, or at least about 10 micrometers or about 20 micrometers in length, and can be less than about 100 nm, less than about 80 nm, less than about 60 nm, less than about 40 nm, less than about 20 nm, less than about 10 nm, or less than about 5 nm in thickness (height and width). The nanoscale wires may have an aspect ratio (length to thickness) of greater than about 2:1, greater than about 3:1, greater than about 4:1, greater than about 5:1, greater than about 10:1, greater than about 25:1, greater than about 50:1, greater than about 75:1, greater than about 100:1, greater than about 150:1, greater than about 250:1, greater than about 500:1, greater than about 750:1, or greater than about 1000:1 or more in some cases.

A "nanowire" (e. g. comprising silicon and/or another semiconductor material) is a nanoscopic wire that is typically a solid wire, and may be elongated in some cases. Preferably, a nanowire (which is abbreviated herein as "NW") is an elongated semiconductor, i.e., a nanoscale semiconductor. A "non-nanotube nanowire" is any nanowire that is not a nanotube. In one set of embodiments of the invention, a non-

nanotube nanowire having an unmodified surface can be used in any arrangement of the invention described herein in which a nanowire or nanotube can be used.

As used herein, a "nanotube" (e.g. a carbon nanotube) is a nanoscopic wire that is hollow, or that has a hollowed-out core, including those nanotubes known to those of ordinary skill in the art. "Nanotube" is abbreviated herein as "NT." Nanotubes are used as one example of small wires for use in the invention and, in certain embodiments, devices of the invention include wires of scale commensurate with nanotubes.

As used herein, an "elongated" article (e.g. a semiconductor or a section thereof) is an article for which, at any point along the longitudinal axis of the article, the ratio of the length of the article to the largest width at that point is greater than 2:1.

As used herein, a "width" of an article is the distance of a straight line from a point on a perimeter of the article, through the center of the article, to another point on the perimeter of the article. As used herein, a "width" or a "cross-sectional dimension" at a point along a longitudinal axis of an article is the distance along a straight line that passes through the center of a cross-section of the article at that point and connects two points on the perimeter of the cross-section. The "cross-section" at a point along the longitudinal axis of an article is a plane at that point that crosses the article and is orthogonal to the longitudinal axis of the article. The "longitudinal axis" of an article is the axis along the largest dimension of the article. Similarly, a "longitudinal section" of an article is a portion of the article along the longitudinal axis of the article that can have any length greater than zero and less than or equal to the length of the article. Additionally, the "length" of an elongated article is a distance along the longitudinal axis from end to end of the article.

As used herein, a "cylindrical" article is an article having an exterior shaped like a cylinder, but does not define or reflect any properties regarding the interior of the article. In other words, a cylindrical article may have a solid interior, may have a hollowed-out interior, etc. Generally, a cross-section of a cylindrical article appears to be circular or approximately circular, but other cross-sectional shapes are also possible, such as a hexagonal shape. The cross-section may have any arbitrary shape, including, but not limited to, square, rectangular, or elliptical. Regular and irregular shapes are also included.

As used herein, an "array" of articles (e.g., nanoscopic wires) comprises a plurality of the articles, for example, a series of aligned nanoscale wires, which may or may not be in contact with each other. As used herein, a "crossed array" or a "crossbar array" is an array where at least one of the articles contacts either another of the articles or a signal node (e.g., an electrode).

Many nanoscopic wires as used in accordance with the present invention are individual nanoscopic wires. As used herein, "individual nanoscopic wire" means a nanoscopic wire free of contact with another nanoscopic wire (but not excluding contact of a type that may be desired between individual nanoscopic wires, e.g., as in a crossbar array). For example, an "individual" or a "free-standing" article may, at some point in its life, not be attached to another article, for example, with another nanoscopic wire, or the free-standing article may be in solution. This is in contrast to nanotubes produced primarily by laser vaporization techniques that produce materials formed as ropes having diameters of about 2 nm to about 50 nm or more and containing many individual nanotubes (see, for example, Thess, *et al.*, "Crystalline Ropes of Metallic Carbon Nanotubes," *Science*, 273:483-486 (1996)). This is also in contrast to conductive portions of articles which differ from surrounding material only by having been altered chemically or physically, *in situ*, i.e., where a portion of a uniform article is made different from its surroundings by selective doping, etching, etc. An "individual" or a "free-standing" article is one that can be (but need not be) removed from the location where it is made, as an individual article, and transported to a different location and combined with different components to make a functional device such as those described herein and those that would be contemplated by those of ordinary skill in the art upon reading this disclosure.

In some embodiments, at least a portion of a nanoscopic wire may be a bulk-doped semiconductor. As used herein, a "bulk-doped" article (e. g. an article, or a section or region of an article) is an article for which a dopant is incorporated substantially throughout the crystalline lattice of the article, as opposed to an article in which a dopant is only incorporated in particular regions of the crystal lattice at the atomic scale, for example, only on the surface or exterior. For example, some articles such as carbon nanotubes are typically doped after the base material is grown, and thus the dopant only extends a finite distance from the surface or exterior into the interior of

the crystalline lattice. It should be understood that "bulk-doped" does not define or reflect a concentration or amount of doping in a semiconductor, nor does it necessarily indicate that the doping is uniform. In particular, in some embodiments, a bulk-doped semiconductor may comprise two or more bulk-doped regions. Thus, as used herein to describe nanoscopic wires, "doped" refers to bulk-doped nanoscopic wires, and, accordingly, a "doped nanoscopic (or nanoscale) wire" is a bulk-doped nanoscopic wire. "Heavily doped" and "lightly doped" are terms the meanings of which are clearly understood by those of ordinary skill in the art. In some cases, one or more regions may comprise a single monolayer of atoms ("delta-doping"). In certain cases, the region may be less than a single monolayer thick (for example, if some of the atoms within the monolayer are absent). As a specific example, the regions may be arranged in a layered structure within the nanoscale wire, and one or more of the regions may be delta-doped or partially delta-doped.

As used herein, the term "Group," with reference to the Periodic Table, is given its usual definition as understood by one of ordinary skill in the art. For instance, the Group II elements include Mg and Ca, as well as the Group II transition elements, such as Zn, Cd, and Hg. Similarly, the Group III elements include B, Al, Ga, In and Tl; the Group IV elements include C, Si, Ge, Sn, and Pb; the Group V elements include N, P, As, Sb and Bi; and the Group VI elements include O, S, Se, Te and Po. Combinations involving more than one element from each Group are also possible. For example, a Group II-VI material may include at least one element from Group II and at least one element from Group VI, for example, ZnS, ZnSe, ZnSSe, ZnCdS, CdS, or CdSe. Similarly, a Group III-V material may include at least one element from Group III and at least one element from Group V, for example GaAs, GaP, GaAsP, InAs, InP, AlGaAs, or InAsP. Other dopants may also be included with these materials and combinations thereof, for example, transition metals such as Fe, Co, Te, Au, and the like.

As used herein, a "semiconductor" is given its ordinary meaning in the art, i.e., an element having semiconductive or semi-metallic properties (i.e., between metallic and non-metallic properties). An example of a semiconductor is silicon. Other non-limiting examples include elemental semiconductors, such as gallium, germanium, diamond (carbon), tin, selenium, tellurium, boron, or phosphorous. The semiconductor may be undoped or doped (e.g., p-type or n-type).

As used herein, a "single crystal" item (e.g., a semiconductor) is an item that has covalent bonding, ionic bonding, or a combination thereof throughout the item. Such a single crystal item may include defects in the crystal, but is distinguished from an item that includes one or more crystals, not ionically or covalently bonded, but merely in close proximity to one another.

The following U.S. provisional and utility patent application documents are incorporated herein by reference in their entirety for all purposes: Serial No. 60/633,733, entitled "Nanoscale Wire Based Data Storage," filed December 6, 2004; Serial No. 60/142,216, entitled "Molecular Wire-Based Devices and Methods of Their Manufacture," filed July 2, 1999; Serial No. 60/226,835, entitled, "Semiconductor Nanowires," filed August 22, 2000; Serial No. 10/033,369, entitled "Nanoscopic Wire-Based Devices and Arrays," filed October 24, 2001, published as Publication No 2002/0130353 on September 19, 2002; Serial No. 60/254,745, entitled, "Nanowire and Nanotube Nanosensors," filed December 11, 2000; Serial No. 60/292,035, entitled "Nanowire and Nanotube Nanosensors," filed May 18, 2001; Serial No. 60/292,121, entitled, "Semiconductor Nanowires," filed May 18, 2001; Serial No. 60/292,045, entitled "Nanowire Electronic Devices Including Memory and Switching Devices," filed May 18, 2001; Serial No. 60/291,896, entitled "Nanowire Devices Including Emissive Elements and Sensors," filed May 18, 2001; Serial No. 09/935,776, entitled "Doped Elongated Semiconductors, Growing Such Semiconductors, Devices Including Such Semiconductors, and Fabricating Such Devices," filed August 22, 2001, published as Publication No. 2002/0130311 on September 19, 2002; Serial No. 10/020,004, entitled "Nanosensors," filed December 11, 2001, published as Publication No. 2002/0117659 on August 29, 2002; Serial No. 60/348,313, entitled "Transistors, Diodes, Logic Gates and Other Devices Assembled from Nanowire Building Blocks," filed November 9, 2001; Serial No. 60/354,642, entitled "Nanowire Devices Including Emissive Elements and Sensors," filed February 6, 2002; Serial No. 10/152,490, entitled, "Nanoscale Wires and Related Devices," filed May 20, 2002; Serial No. 10/196,337, entitled, "Nanoscale Wires and Related Devices," filed July 16, 2002, published as Publication No. 2003/0089899 on May 15, 2003; Serial No. 60/397,121, entitled "Nanowire Coherent Optical Components," filed July 19, 2002; Serial No. 10/624,135, entitled "Nanowire Coherent Optical Components," filed July 21, 2003; Serial No. 60/524,301, entitled,

"Nanoscale Arrays and Related Devices," filed November 20, 2003; Serial No. 60/397,121, entitled "Nanowire Coherent Optical Components," filed December 11, 2003; Serial No. 60/544,800, entitled "Nanostructures Containing Metal-Semiconductor Compounds," filed February 13, 2004; Serial No. 10/347,121, entitled, "Array-Based Architecture for Molecular Electronics," filed January 17, 2003; Serial No. 10/627,405, entitled "Stochastic Assembly of Sublithographic Nanoscale Interfaces," filed July 24, 2003; Serial No. 10/627,406, entitled "Sublithographic Nanoscale Memory Architecture," filed July 24, 2003; Serial No. 60/524,301, entitled "Nanoscale Arrays and Related Devices," filed November 20, 2003; Serial No. 60/551,634, entitled "Robust Nanostructures," filed March 8, 2004; and a patent application entitled "Nanoscale Arrays, Robust Nanostructures, and Related Devices," filed November 22, 2004. The following International Patent Publication is incorporated herein by reference in their entirety for all purposes: Application Serial No. PCT/US00/18138, entitled "Nanoscopic Wire-Based Devices, Arrays, and Methods of Their Manufacture," filed June 30, 2000, published as Publication No. WO 01/03208 on January 11, 2001; Application Serial No. PCT/US01/26298, entitled "Doped Elongated Semiconductors, Growing Such Semiconductors, Devices Including Such Semiconductors, and Fabricating Such Devices," filed August 22, 2001, published as Publication No. WO 02/17362 on February 28, 2002; Application Serial No. PCT/US01/48230, entitled "Nanosensors," filed December 11, 2001, published as Publication No. WO 02/48701 on June 20, 2002; Application Serial No. PCT/US02/16133, entitled "Nanoscale Wires and Related Devices," filed May 20, 2002, published as Publication No. WO 03/005450 on January 16, 2003.

The following examples are intended to illustrate certain embodiments of the present invention, but do not exemplify the full scope of the invention.

EXAMPLE 1

This example demonstrates the synthesis of semiconductor/dielectric oxide/ferroelectric oxide core/shell/shell nanoscale wire structure, specifically p-Si/ZrO_2/$BaTiO_3$ core/shell/shell nanoscale wires (Fig. 1A), according to one embodiment of the invention. In this example, the shells were fabricated using ALD techniques (atomic layer deposition), but other techniques, for example, solution-based approaches, can be used as well.

The synthesis starts from chemical vapor deposition growth of p-type silicon nanoscale wires using gold colloids as a catalyst, silane as a reactant, and diborane as a dopant in the well-known VLS growth process. After growth, the growth wafer was transferred directly into an atomic layer deposition reactor. ZrO_2 high-K dielectric oxide was deposited onto the Si nanoscale wires to make p-Si/ZrO_2 core/shell nanoscale wires by using $ZrCl_4$ as a Zr source and water vapor as an oxygen source. ZrO_2 can function as a high-K dielectric, which can enhance performance of the Si nanoscale wire field-effect transistor by providing a stronger electric field coupling between the Si channel and the metal gate of the transistor. ZrO_2 may also be effective as a diffusion barrier to stop compositional diffusion from $BaTiO_3$ towards Si. ZrO_2 may also help to achieve a longer retention time by reducing the speed of degradation/lose of data stored in $BaTiO_3$ shell (also known as depolarization time). In some cases, ZrO_2 may be chemically etched away, which may allow ohmic contacts to be made with the Si nanoscale wire core. However, in other embodiments, other dielectric oxides can also be used, for example, Al_2O_3 and/or HfO_2, and in some cases, more than one dielectric oxide may be used, for example, ZrO_2 and Al_2O_3, ZrO_2 and HfO_2, etc.

After depositing about 2 nm to about 3 nm of ZrO_2 on the Si nanoscale wire core, the precursors were changed to allow for the deposition of $BaTiO_3$ on the Si/ZrO_2 core/shell nanoscale wires to make the final Si/ZrO_2/$BaTiO_3$ core/shell/shell nanoscale wire. The precursors used in this example were barium bis(pentamethylcyclopentadienyl) as the barium source, titanium tetraisopropoxide as the titanium source, and water vapor as the oxygen source.

Examples of nanoscale wires produced using these techniques are illustrated in Fig. 9. Fig. 9A is a low resolution transmission electron microscope (TEM) image of several Si/ZrO_2/$BaTiO_3$ nanoscale wires. In this image, the Si core thickness was found to be around 20 nm, the ZrO_2 shell thickness was found to be around 2.5 nm, and the $BaTiO_3$ thickness was found to be around 15 nm. A higher resolution TEM image is shown in Fig. 9B. In this figure, the white dashed lines indicate the $BaTiO_3$/ZrO_2 interface (left) and the ZrO_2/Si interface (right). From two-dimensional Fourier transforms of the lattice resolved image shown in Fig. 9B, it was found that tetragonal phase $BaTiO_3$ grew along the (010) direction, with the zone axis at [010] (Fig. 9C). Additionally, tetragonal phase ZrO_2 grew along the (112) direction, with the zone axis at

[110] (Fig. 9D), and cubic phase Si grew along the (110) direction, with the zone axis at [111] (Fig. 9E).

After synthesis, the core/shell/shell nanoscale wires were characterized by elemental mapping. Fig.1C shows a scanning transmission electron microscopy image of the core/shell/shell wire and Fig. 1B shows a line profile of elemental composition of Ba/Ti, Zr, and Si across the wire (transversely). Additional evidence was obtained from elemental mapping measurements, shown in Figs. 1D-1F. Si was present in the core (Fig. 1D), ZrO_2 was present in the inner shell (Fig. 1E), and $BaTiO_3$ was present in the outer shell (Fig. 1F).

Electrostatic force microscopy was used to characterize the ferroelectric behavior of the core/shell/shell wires. In these experiments, a conductive atomic force microscopy tip was used to apply a local electric field on $BaTiO_3$ shell of the $Si/ZrO_2/BaTiO_3$ nanoscale wire, and at the same time, ground the Si nanoscale wire core from the source and the drain. In Fig. 2, the conductance of the Si nanoscale wire was measured, sequentially: before polarizing the wire (using positive voltage) (A), after polarizing the wire (using positive voltage) (B), depolarizing the wire (C), after polarizing the wire (using negative voltage) (D), and depolarization (E). These studies showed that after polarizing the wire using positive voltage, the conductance dropped from about 10^{-7} S to about 10^{-12} S. This polarization could be removed either by naturally depolarizing the wire and/or applying a negative voltage to flip the direction of polarization. Thus, the conductance can be brought back to the original value, or to a higher value.

To demonstrate memory devices based on these $Si/ZrO_2/BaTiO_3$ core/shell/shell nanoscale wires, a FET type device was fabricated with source-drain metal contacts on the Si core by chemically etching the $BaTiO_3$ and ZrO_2 shells away and adding a top metal gate on the $BaTiO_3$ shell, using techniques analogous to MFIS (Metal gate/Ferroelectric oxide/Insulator/Semiconductor) planar devices. Transport data (Fig. 3A) showed that the source-drain contact was ohmic and the source-drain current could be turned off after the applied top-gate voltage exceeded a certain threshold. Additional measurements of conductance vs. top gate voltage (Fig. 3B) showed a large hysteresis, where one can write polarization into $BaTiO_3$ shell with a top gate voltage larger than the +5 V needed to depolarize the nanoscale wire at the off state (i.e., at low conductance). During reading, if the conductance of the transistor is found to be high, this means that

no polarization has been written to the nanoscale wire (e.g., which can be defined to be "0"). However, if the conductance of the transistor is low but it can be increase by applying a pulse of small negative top gate voltage (which is not large enough to remove or alter the polarization), then this means that polarization has been written to the nanoscale wire (e.g., which can be defined to be "1").

In some cases, these nanoscale wires can be used to store multiple bits of data per transistor. To demonstrate this feature, three metal top gates (A, B, and C) were fabricated onto one $Si/ZrO_2/BaTiO_3$ nanoscale wire (Fig. 3C). Initially, the nanoscale wire was polarized with C only, so the data stored in the nanoscale wire was "001." To read this data, pulses of negative voltage were applied to the three top gates in sequence. Fig. 3D shows that only when the voltage is applied to gate C, there is a response of increasing conductance, thus indicating a "1" rather than a "0" in gate C. Similarly, one can also write data to gates A and B; to read this data, pulses of negative voltage can be applied to the three top gates in sequence. It should be noted that no crosstalk was observed between gates A, B, and C. In Fig. 3E, increasing conductance was observed only when pulses of voltage were simultaneously applied to multiple gates. However, until the pulse of negative voltage is applied at gate A and B at the same time, can one see the response of increasing conductance (Fig. 3e), and thus, there was no crosstalk observed among gates A, B and C. These results are summarized in Fig. 3F. Moreover, a large retention time for this data within the nanoscale wire was observed. In Fig. 3G, no obvious degradation-increasing of conductance after the nanoscale wires had been polarized and the wires were "turned off" with low conductance was detected.

Additional data can be seen in Fig. 10. Fig. 10A illustrates transport results of the $Si/ZrO_2/BaTiO_3$ nanoscale wires, measured at -6 V, -4 V, -2 V, 0 V, 2 V, 4 V, and 6 V top gate voltage. The insert is an AFM image of this device. Fig. 10B is a graph showing a hysteresis loop of conductance vs. top gate voltage. This graph shows two states at a top gate voltage of 0 V. Fig. 10C illustrates the results of a writing/erasing pulse cycle for a memory test using another $Si/ZrO_2/BaTiO_3$ nanoscale wire. Writing to the wire was performed using 5 V with a 100 ns pulse. Monitoring (reading) the conductance change was performed for 150 microsiemans (μS), and erasing was performed at -5 V with a 100 ns pulse, followed by another 150 microsiemans (μS) monitoring (reading) of the conductance change. The insert shows the shape of the 100

ns pulse. Fig. 10D illustrates the conductance change as a result of a writing/erasing pulse showing that memory made by $Si/ZrO_2/BaTiO_3$ nanowires can be operated with a speed of at least 100 ns, which correspond to 10 Mb/s, faster than the speed of a commercial USB2 flash memory drive. Faster speeds, such as 50 nS (20 Mb/s), were also observed in other experiments (data not shown). The graph in Fig. 10E is a retention test of the memory device over a 1-week time period. No significant changes in conductance were observed. Fig. 10F is an electrostatic force microscopy (EFM) image of a device using an 80nm $Si/ZrO_2/BaTiO_3$ nanoscale wire (30 nm core + 25 nm shells), fabricated using techniques similar to those described above, showing a correlation between polarization and conductance. The left image shows the device without any polarization in the $BaTiO_3$ shell, showing a normally "on" state in conductance. The middle image shows the device, using a positive voltage on an atomic force microscope (AFM) tip to write the polarization into the shell to "turn off" the device. The right image shows the device, using a negative voltage on an AFM tip to write the polarization into the shell to "turn on" the device again.

Dense arrays of nanoscale wires are also possible, as ferroelectric states can persist down to the domain thickness of 1.2 nm. In some cases, other nanowires, for example NiSi nanowires as discussed in U.S. Provisional Patent Application Serial No. 60/544,800, filed February 13, 2004, entitled "Nanostructures Containing Metal-Semiconductor Compounds," by Lieber, *et al.*, or International Patent Application Serial No. PCT/US2005/004459 filed February 14, 2005, entitled "Nanostructures Containing Metal Semiconductor Compounds," by Lieber, *et al.*, each incorporated herein by reference, may be crossed with the $Si/ZrO_2/BaTiO_3$ nanoscale wires to achieve a high density for data storage.

EXAMPLE 2

This example illustrates the fabrication of silicon-functional oxide core-shell nanowire heterostructures by atomic layer deposition (ALD), in which the conformal coating of various materials, including oxides, on silicon nanowires was achieved through cycled self-limiting surface reactions by alternating pulse and purge cycles for different reactants. The thickness of the coating was controlled by the number of deposition cycles down to the atomic scale, and thus, the technique may be suitable for fabricating multi-compositional heterostructures with clean interfaces.

One of the example structures synthesized was a silicon (Si)–zirconium oxide (ZrO_2)–barium titanate ($BaTiO_3$) semiconductor-dielectric oxide-ferroelectric oxide core-shell-shell nanowire heterostructure (Fig. 12). Fig. 12A shows the deposition of functional oxide shells over p-type silicon nanowires. The synthesis started from the growth of p-type Si nanowires by chemical vapor deposition, followed by vapor phase atomic layer depositions of ZrO_2 and $BaTiO_3$ shells with well-controlled deposition rates of 0.03 nm $cycle^{-1}$ for ZrO_2 (Fig. 12A, lower line) and 0.05 nm $cycle^{-1}$ for $BaTiO_3$ (Fig. 12A, upper line).

P-type Si nanowires were synthesized via chemical vapor deposition using monodisperse gold nanoclusters (Ted Pella, Inc., Redding, CA) as catalysts, silane (SiH_4) as a vapor-phase reactant, and diborane (B_2H_6) as a dopant precursor. Following synthesis, the growth substrate with uniform diameter, free-standing Si nanowires was loaded into an ASM Microchemistry F120 atomic layer deposition system followed by deposition of ZrO_2 and then $BaTiO_3$. Zirconium chloride ($ZrCl_4$) was used as the precursor for ZrO_2. Barium bis(pentamethylcyclopentadienyl) ($Ba(C_5Me_5)_2$) and titanium tetraisopropoxide ($Ti(O\text{-}i\text{-}Pr)_4$) were used as precursors for $BaTiO_3$. In both cases, water (H_2O) vapor was used as oxygen source. After the depositions, the substrate was annealed at 800 °C in a tube furnace for 30 minutes. The annealing was carried out in oxygen with flow rate of 200 sccm (standard cubic centimeters per minute) at pressure of 450 Torr.

Transmission electron microscopy (TEM) studies (Fig. 12B) of the samples prepared in this manner showed nanowires with generally uniform diameters and lengths of up to tens of micrometers. For instance, in Fig. 12B, the core-shell nanowire heterostructures had an average diameter of about 60 nm (25 nm Si core, 2.5 nm ZrO_2 shell, and 15 nm $BaTiO_3$ shell). The scale bar is 200 nm.

The diametrical contrast observed in the TEM images (Figs. 12B, 12C, and 12D) as well as scanning TEM (STEM) images (Fig. 12F) may be indicative of a core-shell structure. Fig. 12C is a low magnification TEM projection view of a typical core-shell nanowire. The dashed-line box indicates the view of the TEM image shown in Fig. 12D. The scale bar in Fig. 12C is 10 nm. Fig. 12D shows an HRTEM (High Resolution Transmission Electron Microscopy) projection view of the polycrystalline shell of the nanowire heterostructure, with white dashed lines roughly indicating the crystalline

domain boundaries, which are determined by selective-area 2DFT and inverse 2DFT of the shell. The scale bar is 10 nm. High-resolution projection view of the nanowire edge (Fig. 12D) showed a polycrystalline $BaTiO_3$ shell with multiple domains. The domain boundaries (Fig. 12D, white dashed lines) could be roughly identified by selective-area two-dimensional Fourier transforms (2DFT) and inverse Fourier transforms of the TEM image (Figs. 12J-12M). Fig. 12J is a 2DFT of domain 1 in Fig. 12D, showing that it aligned with zone axis of (010); Fig. 12C is a 2DFT of domain 2 in Fig. 12D, showing that it aligned with zone axis of $(0\bar{1}1)$; Fig. 12D is a 2DFT of domain 3, showing that it aligned with zone axis of (243); and Fig. 12E is a 2DFT of the domain 4, showing that it aligned with zone axis of (001). Additionally, Fig. 13A shows a 2DFT of the $BaTiO_3$ region with the zone axis of $(0\bar{1}0)$, Fig. 13B shows a 2DFT of the ZrO_2 region with the zone axis of (110), and Fig. 13D shows a 2DFT of the Si region with the zone axis of (111).

Further detailed examination of microtomed cross sections of the core-shell nanowire heterostructures by high-resolution TEM (Fig. 12E) demonstrated that the fabrication yielded abrupt interfaces (Fig. 12H, white dashed line) between the $BaTiO_3$ (left) and ZrO_2 (middle) shells, and the Si (right) core regions with zone axes of $BaTiO_3$, ZrO_2. For example, Fig. 12E is an HRTEM image of the cross section of the microtomed core-shell nanowire heterostructure, with white dashed lines indicating the interfaces among crystalline $BaTiO_3$ (left), ZrO_2 (middle) and Si (right) regions with the zone axes of $BaTiO_3$, ZrO_2, and Si to be $(0\bar{1}0)$, (110), and (111) respectively, from 2DFT of the TEM image. The insets illustrate crystal structures simulations of the $BaTiO_3$ (left), ZrO_2 (center), and Si (right) regions along the zone axes showing the consistency with the lattice-resolved image. The scale bar in Fig. 12E is 2 nm.

The zone axes were further confirmed by the consistency between the crystal structures simulations (insets, Fig. 12E) and the lattice-resolved image. ZrO_2, which crystallized at relatively lower temperature, served as a diffusion barrier during post-annealing to optimize the interface between the ferroelectric oxide and the semiconductor. Furthermore, energy dispersive X-ray spectroscopy (EDX) performed on the sample confirmed the elemental spatial distribution, showing that Si was localized at the core (Fig. 12G), Zr at the inner shell (Fig. 12H), and Ba and Ti at the outer shell

(Fig. 12I). Figs. 12F-12I are EDX elemental mappings of the core-shell nanowire heterostructure performed by STEM (Scanning Transmission Electron Microscopy). Fig. 12F is a STEM image of a ~122 nm core-shell nanowire heterostructure prepared using ~37 nm Si nanowire as a core with a ~2.5 nm ZrO_2 shell and a ~40 nm $BaTiO_3$ shell. The larger core diameter and thicker shell were used here for EDX characterization purposes. In these figures, Si was localized at the core (Fig. 12D), Zr at the inner shell (Fig. 12E), and Ba and Ti at the outer shell (Fig. 12F). The scale bars in Figs. 12F-12I are each 50 nm.

EXAMPLE 3

This example illustrates the synthesis of a well-defined semiconductor-functional oxide core-shell nanowire heterostructure with a clean interface. In this example, a field-effect transistor (FET) device was prepared based on a $Si/ZrO_2/BaTiO_3$ core-shell nanowire heterostructure (Fig. 14). To form the device, the oxides at the source-drain regions were etched away by hydrogen fluoride (HF) acid, followed by deposition of metal contacts on the p-type Si core. A nickel top gate was fabricated between the source-drain contacts on top of the $BaTiO_3$ shell (inset, Fig. 14A, which is a SEM image showing the device geometry, and source-drain contacts having 3 micrometer separation on the p-type Si nanowire core and an 800 nm wide top gate on the top of the $BaTiO_3$ shell in the middle of the channel). The scale bar in the inset is 2 micrometers. Transport results of current (I_{sd}) versus source-drain voltage (V_{sd}) data (Fig. 14A) at different gate voltages (V_{gs}) obtained from a core-shell nanowire with a total diameter of ~60 nm (25 nm Si core, 2.5 nm ZrO_2 shell, and 15 nm $BaTiO_3$ shell) exhibited the behavior expected of a depletion mode p-FET. Fig. 14A illustrates exemplary characteristics for a 60 nm core-shell nanowire heterostructure transistor at different top gate voltage (from bottom to top: -4 V to +6 V, 2 V intervals).

Further measurements of the source-drain conductance versus gate voltage a bias voltage of -1.5 V showed a hysteresis loop in the gate sweep (Fig. 14B). In the hysteresis loop, two bi-stable states were observed around 0 V gate voltages: one at a higher conductive "on" state, and one at a lower conductive "off" state. Switching from "on" to "off" occurred at +5 V, whereas the reverse process occurred at -3 V.

To show that the origin of the hysteresis loop was polarization switching in ferroelectric $BaTiO_3$, electrostatic force microscopy (EFM) measurements were

performed on the FET devices without a top gate (Fig. 14C). In Fig. 14C, EFM measurement performed on a FET device without top gate showed that a ferroelectric polarization was generated on the $BaTiO_3$ shell by a gate voltage applied to the conductive AFM tip, which existed until a large enough opposite gate voltage was applied that was sufficient to "flip" the direction of the polarization. The scale bars are 2 micrometers.

In the EFM measurements, a conductive AFM tip was used (silicon coated with Pt/Ir) as a local gate to replace the metal top gate. The device was grounded and scanned at the tip voltage to write polarization from -25 V to +25 V and then back to -25 V with 5 V intervals. The tip was kept at a constant height of 6 nm above the topological features during the writing. For EFM imaging of the polarization status, the device was also grounded and the tip was kept at +2 V with a constant height of 30 nm above the topological features. The electrostatic interaction between the $BaTiO_3$ shell and the tip was sensed by the shift of resonant frequency of the tip cantilever. After writing at every data point, the device was biased at -1 V to monitor the conductance change.

These results generally showed that a ferroelectric polarization was locally generated in the $BaTiO_3$ shell by a gate voltage applied on the conductive atomic force microscope (AFM) tip, which was retained until a sufficiently large opposite gate voltage was applied to flip the direction of the polarization. In these experiments, because a positive gate voltages was used to turn "off" the p-type FET device that was normally "on" at large conductances, the two polarization states, which corresponded to the bi-stable states at the gate sweep at 0 V gate voltage, were arbitrarily assigned as "0" for the state with high conductance "on" state (upper inset, Fig. 14C) and "1" for the low conductance "off" state (lower inset, Fig. 14C). The core-shell nanowire heterostructure FET, once turned "off" by the ferroelectric polarization generated by a positive gate voltage, was able to stay in the "off" state for weeks without obvious degradation (lower spots), even after the removal of the external positive gate voltage (Fig. 14D), thereby demonstrating device non-volatility. Similarly, monitoring of the conductance change of a FET device over weeks showed no obvious degradation of the "on" state conductance (upper spots).

The switching speed and endurance of the core-shell nanowire heterostructure FET device was also characterized (Fig. 14E). These characteristics may be useful for

determining the viability of such nanowire structures in integrated non-volatile memory arrays. To measure the switching speed and endurance of the FET device, an Agilent 33220A function and arbitrary waveform generator was connected to the top gate, which gave operation pulses width of 100 ns and amplitude of +7 V and -7 V (actual output +5 V and -5 V at high frequency as measured separately) as writing and erasing pulses in an alternative manner with 150 microsecond interval. The conductance of the FET device was monitored simultaneously through current amplifier, which gave an intrinsic instrument response of 15 microseconds, even when all the filters were turned off. For the endurance measurements, the FET device was continuously switched "on" and "off" using the pulses for one hour with fixed bias at -1 V, which gave an endurance of at least 10^7 cycles.

An FET device based on the heterostructure discussed above showed that the writing/erasing speed of the ferroelectric polarization was at least 100 ns, using pulses generated by a waveform function generator (insets, Fig. 14E), which were able to switch the FET either "on" or "off." Faster switching speeds of 50 ns were also observed.

The switching behavior was retained without obvious fatigue degradation, even after 10^7 cycles of writing and erasing (Fig. 14E). The fast switching speed, as well as the long endurance observed in the device, was comparable to planar ferroelectric random access memory devices and superior to many commercially-available flash memories, which typically shows switching speeds of microsecond time scales and endurances of 10^5 cycles. It is believed that the noise level in the conductance switching data (Fig. 14E) mainly arose from the fact that all of the noise filters were turned off in the current amplifier to achieve the fastest instrument response, which sets an instrumental limit for the reading speed to be 15 microseconds. In fact, even higher reading speeds may be possible. The intrinsic switching speed of the ferroelectric oxides is believed to be on the picosecond time scale, and the writing/erasing/reading speeds observed here were only limited by the RC delay in the measurement circuit, not in the device itself.

This is illustrated in more detail in Fig. 15. In this figure, the current amplifier in the measurement circuit was found to set a response limit for the reading speed at 15 microseconds. Fig. 15A is a comparison between the square wave (upper line) generated

by function generator and the signal read through the current amplifier (lowerline) in the measurement circuit, showing the 15 microsecond delay. Fig. 15B shows that the switching speed measurements of the core-shell nanowire heterostructure FET memory device appeared to have the same 15 microsecond delay in read response after a writing/erasing pulse is applied; thus, the read speed was limited by the instrument response, not by the response of the core-shell nanowire heterostructure FET memory device.

Figs. 14F and 14G illustrate operation pulses width of 100 ns and amplitude of +7 V and -7 V (actual output +5 V and -5 V at high frequency as measured separately), applied to the top gate and used as writing and erasing pulses in an alternative manner with 150 microsecond intervals to switch "off" and "on" the FET memory device. The device could be switched "on" and "off" continuously for one hour with a fixed -1 V source-drain bias without obvious fatigue, showing an endurance of at least 10^7 cycles (Fig. 14E).

EXAMPLE 4

In this example, for the FET-type memory devices based on ferroelectric oxide, the critical thickness for the ferroelectric oxides and the minimum gate width/pitch were examined. To address the first issue, core-shell nanowire heterostructures with thinner $BaTiO_3$ shells were fabricated. Transport measurements (data not shown) showed that when the thickness of $BaTiO_3$ shell was decreased to 10 nm, the expected depolarizing electrostatic field caused by dipoles at the ferroelectric oxide-metal gate interfaces substantially diminished the ferroelectric properties of the oxides. However, this can be overcome using strained perovskite oxide superlattice structures, which may reduce the critical thickness down to single–unit cell level.

A series of devices were fabricated with different gate widths from 500 nm to 20 nm (Fig. 16). The devices were prepared with different gate widths as follows: Fig. 16A, 500 nm; Fig. 16B, 200 nm; Fig. 16C, 50 nm; and Fig. 16D, 20 nm. The scale bars are 500 nm for Figs. 16A and 16B, and 250 nm for Figs. 16C and 16D.

The results from these experiments showed that the switching behavior was retained even with a 20 nm wide metal gate (Fig. 16D). The on-off ratio increased up to eight orders of magnitude with decreasing gate widths (left arrow, Fig. 16E), which appeared to be the result of less leakage current from the gate to the channel (right arrow, Fig.

16E). The writing/erasing voltage window (-3 V ~ +5 V) was found to be similar for these devices, suggesting that all of these switching behaviors were due to ferroelectric polarization in $BaTiO_3$ shell. These experiment results also showed that a writing polarization using a +8 V positive gate voltage (middle line) on gate A turned off the FET device (lower line), which was not turned back "on" by a -9 V erasing voltage applied to gate B (upper line), suggesting substantially no crosstalk between the two adjacent gates. With no crosstalk between the two domains beneath two adjacent 50 nm wide metal gates with 100 nm pitch (Fig. 16F), an integration density of at least 15 Gbits/cm^2 was thereby demonstrated as being achievable. The inset in Fig. 16F is an SEM image of a FET device with two adjacent 50 nm wide metal gates (A and B) with 100 nm pitch. The scale bar is 200 nm.

EXAMPLE 5

The above examples suggest that different ferroelectric polarizations can exist on different domains in a small region of the nanowires without crosstalk, and their polarization statuses can still be distinguished individually. A device having these characteristics was prepared in this example (Fig. 17).

Specifically, multiple gates crossing one FET devices were fabricated (Fig. 17A) to store multiple bits of data per transistor, which expands on the conventional configuration in which only one bit can be stored per transistor. The inset in Fig. 17A shows an SEM of an FET memory device with multiple gates. The scale bar in the inset is 2 micrometers. These results, in summary, showed that one can randomly write different combinations of polarization using a positive gate voltage applied on the metal gate; for example, applying +8 V on all three gates on the FET (Fig. 17A) will write polarizations in the separate $BaTiO_3$ domains beneath the gates, which will turn off the device and allow for multiple bits of data ("111") to be stored (Fig. 17B, line ABC). To read the data, a small negative gate voltage (usually -1 V), which was large enough to screen part of the electric field caused by the ferroelectric polarization and increase the conductance, but small enough not to reverse the ferroelectric polarization direction, was applied to all three gates. In this way, one can observe the maximum conductance increase from the "off" state (Fig. 17B, line ABC) but not with other combinations with mismatch (Fig. 17B, lines A, B, C, AB, BC and AC). After the reading, the conductance

of the device decreased back to the original "off" state, showing that the process of reading does not appear to disturb the polarization in the ferroelectric oxide.

Using a similar approach, one can also store other combinations, such as 001, 110, etc., to the memory array, and correctly read them out. Further calculations (not shown) showed that the number of the distinguishable bits of data per transistor can be determined by the magnitude difference in the readout conductance between the fully correct readout and one mismatch, which can be extended by further optimizing FET performance. Moreover, this FET device with multiple gates may be considered as non-volatile NOR logic with multiple inputs, in which any input (polarizations created by positive gate voltage, regarded as "1") will turn off the conducting channel and result the output (source voltage) to be low ("0").

Additionally, several devices were prepared to integrate these core-shell nanowire heterostructures into large scale memory arrays and NOR logic device arrays by fabricating multiple gates crossing multiple well-aligned nanowires. However, during the writing procedure, the positive electric field applied on one gate could write polarizations into all the nanowires crossing the gate. To ensure that these cross points were individually addressable, compensation voltages were applied during writing. The function of the compensation voltages applied on both nanowires and gates was to create a relatively small potential drop cross the ferroelectric oxide to avoid any extra writing or disturbance to the possible existence of polarizations at other cross points.

For example, in a memory array (right inset, Fig. 17C) composed of 4 nanowires (W_1, W_2, W_3, W_4) crossing six gates (A, B, C, D, E, F) (left inset, Fig. 17C), applying a +8 V gate voltage on gate B and ground on nanowire W_1 could write polarization at the cross point between nanowire W_1 and gate B, which would turn "off" nanowire W_1 in the device, as shown in Fig. 17C, which is an SEM image of a prototype of cross point memory array with NOR logic, composed of four vertically-aligned nanowires with six crossing metal gates. The scale bar is 200 nm. For the NOR logic measurement, the voltage applied on metal gates was used as input. The V_{sd} was constantly biased at 1 V. A 1 megohm (MΩ) resistor was linked between FET source and ground in series. The voltage drop across the resistor was regarded as output.

The left inset in Fig. 17C is a scheme of the array showing that a strategy of applying writing and compensation voltages on nanowires and metal gates could be used

to address the cross point between nanowire W_1 and gate B without writing extra polarization at the cross points among gate B and nanowires W_2, W_3, W_4. After writing, nanowire W_1 in the device was turned "off" (i.e., a decrease in conductance). However, +6 V on nanowires W_2, W_3, W_4, and +3 V on gates A, C, D, E, F should be applied to avoid writing extra polarization at the cross points among gate B and nanowires W_2, W_3, W_4. The -3 V potential difference between the gates A, C, D, E, and F (+3 V), and nanowires W_2, W_3, W_4 (+6 V) did not appear to wipe the possible existence of polarizations at cross points among them.

A similar strategy was also adopted during the following writing of the cross point between nanowire W_3 and gate E (red point in the inset, in Fig. 17D) without writing extra polarization at the cross points among gate E and nanowires W_1, W_2, W_4, as well as avoiding disturbance to the existing polarization at the cross point between nanowire W_1 and gate B. After writing, nanowire W_3 in the device was turned "off" (upper-line, showing a decrease in conductance, Fig. 17D) while no disturbance was observed on nanowire W_1 in the device (lower line, Fig. 17D).

These results show that such strategy of applying writing and compensation voltage was efficient and allowed individual addressing of the cross points in the array. Further statistical analysis (Fig. 17E) showed that the threshold voltages for writing and erasing may have narrow distributions in some cases, with 4.62±0.08 V for writing (right bars, Fig. 17E) and -3.19±0.06 V for erasing (left bars, Fig. 17E), thereby demonstrating uniformity and reliability of the device arrays.

While several embodiments of the present invention have been described and illustrated herein, those of ordinary skill in the art will readily envision a variety of other means and/or structures for performing the functions and/or obtaining the results and/or one or more of the advantages described herein, and each of such variations and/or modifications is deemed to be within the scope of the present invention. More generally, those skilled in the art will readily appreciate that all parameters, dimensions, materials, and configurations described herein are meant to be exemplary and that the actual parameters, dimensions, materials, and/or configurations will depend upon the specific application or applications for which the teachings of the present invention is/are used. Those skilled in the art will recognize, or be able to ascertain using no more than routine

experimentation, many equivalents to the specific embodiments of the invention described herein. It is, therefore, to be understood that the foregoing embodiments are presented by way of example only and that, within the scope of the appended claims and equivalents thereto, the invention may be practiced otherwise than as specifically described and claimed. The present invention is directed to each individual feature, system, article, material, kit, and/or method described herein. In addition, any combination of two or more such features, systems, articles, materials, kits, and/or methods, if such features, systems, articles, materials, kits, and/or methods are not mutually inconsistent, is included within the scope of the present invention.

All definitions, as defined and used herein, should be understood to control over dictionary definitions, definitions in documents incorporated by reference, and/or ordinary meanings of the defined terms.

The indefinite articles "a" and "an," as used herein in the specification and in the claims, unless clearly indicated to the contrary, should be understood to mean "at least one."

The phrase "and/or," as used herein in the specification and in the claims, should be understood to mean "either or both" of the elements so conjoined, i.e., elements that are conjunctively present in some cases and disjunctively present in other cases. Multiple elements listed with "and/or" should be construed in the same fashion, i.e., "one or more" of the elements so conjoined. Other elements may optionally be present other than the elements specifically identified by the "and/or" clause, whether related or unrelated to those elements specifically identified. Thus, as a non-limiting example, a reference to "A and/or B", when used in conjunction with open-ended language such as "comprising" can refer, in one embodiment, to A only (optionally including elements other than B); in another embodiment, to B only (optionally including elements other than A); in yet another embodiment, to both A and B (optionally including other elements); etc.

As used herein in the specification and in the claims, "or" should be understood to have the same meaning as "and/or" as defined above. For example, when separating items in a list, "or" or "and/or" shall be interpreted as being inclusive, i.e., the inclusion of at least one, but also including more than one, of a number or list of elements, and, optionally, additional unlisted items. Only terms clearly indicated to the contrary, such

as "only one of" or "exactly one of," or, when used in the claims, "consisting of," will refer to the inclusion of exactly one element of a number or list of elements. In general, the term "or" as used herein shall only be interpreted as indicating exclusive alternatives (i.e. "one or the other but not both") when preceded by terms of exclusivity, such as "either," "one of," "only one of," or "exactly one of." "Consisting essentially of", when used in the claims, shall have its ordinary meaning as used in the field of patent law.

As used herein in the specification and in the claims, the phrase "at least one," in reference to a list of one or more elements, should be understood to mean at least one element selected from any one or more of the elements in the list of elements, but not necessarily including at least one of each and every element specifically listed within the list of elements and not excluding any combinations of elements in the list of elements. This definition also allows that elements may optionally be present other than the elements specifically identified within the list of elements to which the phrase "at least one" refers, whether related or unrelated to those elements specifically identified. Thus, as a non-limiting example, "at least one of A and B" (or, equivalently, "at least one of A or B," or, equivalently "at least one of A and/or B") can refer, in one embodiment, to at least one, optionally including more than one, A, with no B present (and optionally including elements other than B); in another embodiment, to at least one, optionally including more than one, B, with no A present (and optionally including elements other than A); in yet another embodiment, to at least one, optionally including more than one, A, and at least one, optionally including more than one, B (and optionally including other elements); etc.

It should also be understood that, unless clearly indicated to the contrary, in any methods claimed herein that include more than one step or act, the order of the steps or acts of the method is not necessarily limited to the order in which the steps or acts of the method are recited.

In the claims, as well as in the specification above, all transitional phrases such as "comprising," "including," "carrying," "having," "containing," "involving," "holding," "composed of," and the like are to be understood to be open-ended, i.e., to mean including but not limited to. Only the transitional phrases "consisting of" and "consisting essentially of" shall be closed or semi-closed transitional phrases,

respectively, as set forth in the United States Patent Office Manual of Patent Examining Procedures, Section 2111.03.

What is claimed is:

CLAIMS

1. An electronic data storage device, comprising:

a first electrode;

a second electrode;

a semiconductive material defining an electrical pathway between the first and second electrodes;

a material proximate the semiconductive material, switchable between at least a first polarization state and a second polarization state,

wherein the semiconductive material is switchable between a first conductive state and a second conductive state in response to the first or second polarization states of the ferroelectric oxide material, respectively, providing conductivity between the first and second electrodes, respectively, of a first conductivity and a second conductivity at least 1000 times the first conductivity.

2. The electronic data storage device of claim 1, wherein the material proximate the semiconductive material comprises a ferroelectric oxide material.

3. The electronic data storage device of claim 1, wherein the semiconductive material comprises a Group IV semiconductor.

4. The electronic data storage device of claim 1, wherein the semiconductive material comprises an elemental semiconductor.

5. The electronic data storage device of claim 1, wherein the semiconductive material comprises Si.

6. The electronic data storage device of claim 1, wherein the semiconductive material comprises a Group III-Group V semiconductor.

7. The electronic data storage device of claim 1, wherein the semiconductive material comprises a p-type dopant.

8. The electronic data storage device of claim 1, wherein the semiconductive material comprises an n-type dopant.

9. The electronic data storage device of claim 1, wherein the ferroelectric oxide material comprises Ba.

10. The electronic data storage device of claim 1, wherein the ferroelectric oxide material comprises a barium titanate.

11. The electronic data storage device of claim 1, wherein the ferroelectric oxide material comprises Zr.

12. The electronic data storage device of claim 1, wherein the ferroelectric oxide material comprises a lead zirconium titanate.

13. The electronic data storage device of claim 1, wherein the ferroelectric oxide material comprises Sr.

14. The electronic data storage device of claim 1, wherein the ferroelectric oxide material comprises a strontium bismuth tantalate.

15. The electronic data storage device of claim 1, wherein the semiconductive material comprises at least one portion having a smallest width of less than about 1 micrometer.

16. The electronic data storage device of claim 15, wherein the semiconductive material comprises at least one portion having a smallest width of less than about 500 nanometers.

17. The electronic data storage device of claim 16, wherein the semiconductive material comprises at least one portion having a smallest width of less than about 200 nanometers.

18. The electronic data storage device of claim 17, wherein the semiconductive material comprises at least one portion having a smallest width of less than about 100 nanometers.

19. The electronic data storage device of claim 18, wherein the semiconductive material comprises at least one portion having a smallest width of less than about 50 nanometers.

20. The electronic data storage device of claim 19, wherein the semiconductive material comprises at least one portion having a smallest width of less than about 30 nanometers.

21. The electronic data storage device of claim 20, wherein the semiconductive material comprises at least one portion having a smallest width of less than about 10 nanometers.

22. The electronic data storage device of claim 1, wherein the ferroelectric oxide material comprises at least one portion having a smallest width of less than about 1 micrometer.

23. The electronic data storage device of claim 22, wherein the ferroelectric oxide material comprises at least one portion having a smallest width of less than about 500 nanometers.

24. The electronic data storage device of claim 23, wherein the ferroelectric oxide material comprises at least one portion having a smallest width of less than about 200 nanometers.

25. The electronic data storage device of claim 24, wherein the ferroelectric oxide material comprises at least one portion having a smallest width of less than about 100 nanometers.

26. The electronic data storage device of claim 25, wherein the ferroelectric oxide material comprises at least one portion having a smallest width of less than about 50 nanometers.

27. The electronic data storage device of claim 26, wherein the ferroelectric oxide material comprises at least one portion having a smallest width of less than about 30 nanometers.

28. The electronic data storage device of claim 27, wherein the ferroelectric oxide material comprises at least one portion having a smallest width of less than about 10 nanometers.

29. The electronic data storage device of claim 1, wherein the ferroelectric oxide material at least surrounds at least a portion of the semiconductive material.

30. The electronic data storage device of claim 29, wherein the semiconductive material defines a core, and the ferroelectric oxide material defines first shell at least partially surrounding the core

31. The electronic data storage device of claim 30, wherein the first shell concentrically surrounds the core.

32. The electronic data storage device of claim 30, wherein the portion of the nanoscale wire comprising the core and the first shell is cylindrical.

33. The electronic data storage device of claim 30, wherein the portion of the nanoscale wire comprising the core and the first shell is faceted.

34. The electronic data storage device of claim 30, wherein the nanoscale wire further comprises a second shell surrounding at least a portion of the core.

35. The electronic data storage device of claim 34, wherein the second shell is positioned between the first shell and the core.

36. The electronic data storage device of claim 34, wherein the second shell comprises a metal oxide.

37. The electronic data storage device of claim 34, wherein the second shell has a dielectric constant of at least about 15.

38. The electronic data storage device of claim 37, wherein the second shell has a dielectric constant of at least about 20.

39. The electronic data storage device of claim 38, wherein the second shell has a dielectric constant of at least about 25.

40. The electronic data storage device of claim 34, wherein the second shell comprises Zr.

41. The electronic data storage device of claim 40, wherein the second shell comprises ZrO2.

42. The electronic data storage device of claim 40, wherein the second shell comprises ZrSiO4.

43. The electronic data storage device of claim 34, wherein the second shell comprises Hf.

44. The electronic data storage device of claim 43, wherein the second shell comprises HfO2.

45. The electronic data storage device of claim 43, wherein the second shell comprises HfSiO4.

46. The electronic data storage device of claim 34, wherein the second shell comprises Al2O3.

47. The electronic data storage device of claim 34, further comprising a third shell surrounding at least a portion of the core.

48. The electronic data storage device of claim 47, wherein the third shell is positioned between the first shell and the second shell.

49. The electronic data storage device of claim 47, wherein the third shell comprises a metal.

50 The electronic data storage device of claim 47, wherein the third shell comprises a noble metal.

51. The electronic data storage device of claim 47, wherein the third shell comprises Pt.

52. The electronic data storage device of claim 1, wherein the second conductivity is at least 10,000 times the first conductivity.

53. The electronic data storage device of claim 1, wherein the second conductivity is at least 100,000 times the first conductivity.

54. An article, comprising:

a nanoscale wire comprising a core and a shell at least partially surrounding the core, wherein the core is semiconductive or conductive, and the shell comprises a ferroelectric oxide material.

55. The article of claim 54, wherein the core is semiconductive.

56. The article of claim 54, wherein the core comprises Si.

57. The article of claim 54, wherein the ferroelectric oxide material comprises Ba.

58. The article of claim 54, wherein the ferroelectric oxide material comprises a barium titanate.

59. The article of claim 54, wherein the nanoscale wire comprises at least one portion having a smallest width of less than about 1 micrometer.

60. The article of claim 54, wherein the nanoscale wire further comprises a second shell surrounding at least a portion of the core.

61. The article of claim 60, wherein the second shell is positioned between the shell and the core.

62. The article of claim 60, wherein the second shell comprises a metal oxide.

63. The article of claim 60, wherein the second shell has a dielectric constant of at least about 15.

64. The article of claim 60, wherein the second shell comprises Zr.

65. The article of claim 64, wherein the second shell comprises ZrO_2.

66. The article of claim 60, further comprising a third shell surrounding at least a portion of the core.

67. The article of claim 66, wherein the third shell is positioned between the shell and the second shell.

68. The article of claim 66, wherein the third shell comprises a metal.

69. The article of claim 66, wherein the third shell comprises a noble metal.

70. The article of claim 66, wherein the third shell comprises Pt.

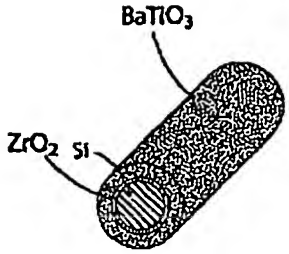


Fig. 1a

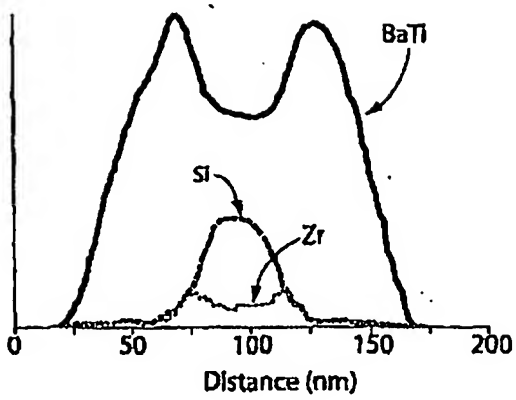


Fig. 1b

Fig. 1c

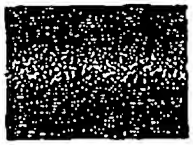


Fig. 1d

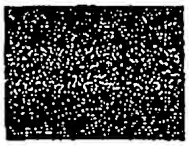


Fig. 1e

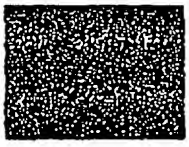


Fig. 1f

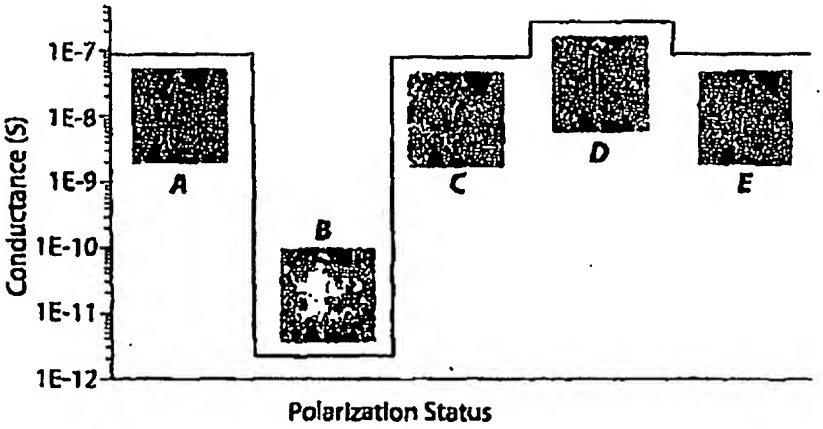


Fig. 2

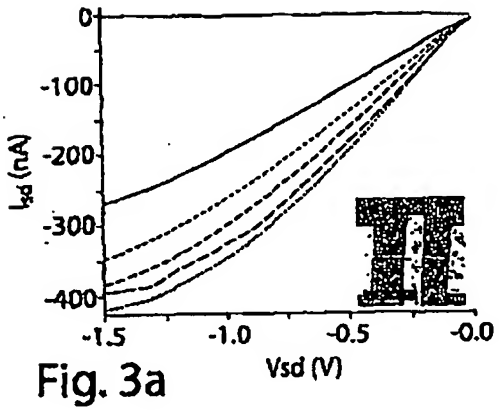


Fig. 3a

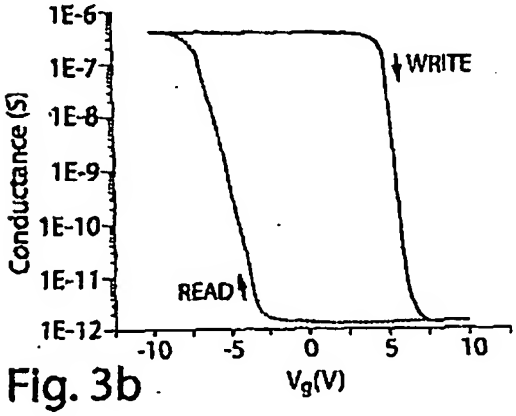


Fig. 3b

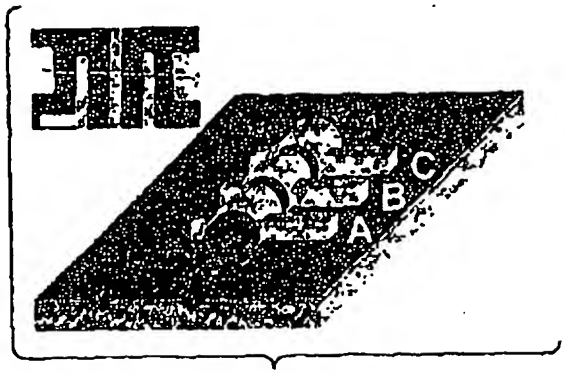


Fig. 3c

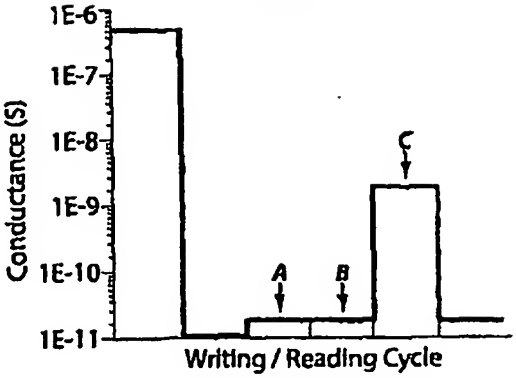


Fig. 3d

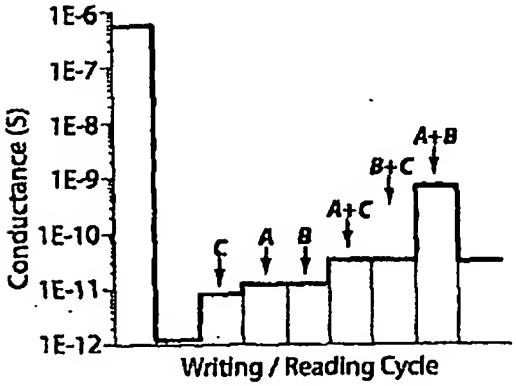


Fig. 3e

	A	B	C	Conductance
Write	0	0	1	Low
Read	1	0	0	Low
Read	0	1	0	Low
Read	0	0	1	High
Write	1	1	0	Low
Read	0	0	1	Low
Read	1	0	0	Low
Read	0	1	0	Low
Read	1	0	1	Low
Read	0	1	1	Low
Read	1	1	0	High

Fig. 3f

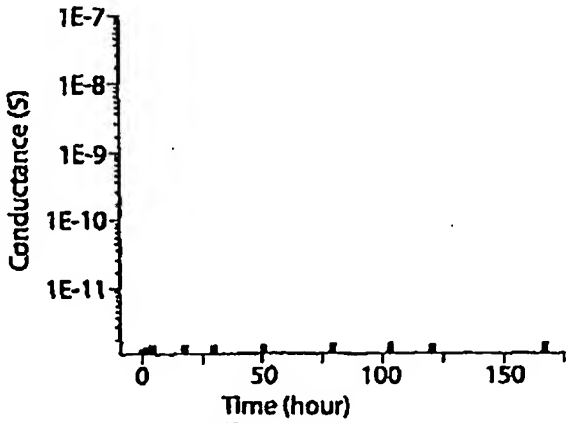


Fig. 3g

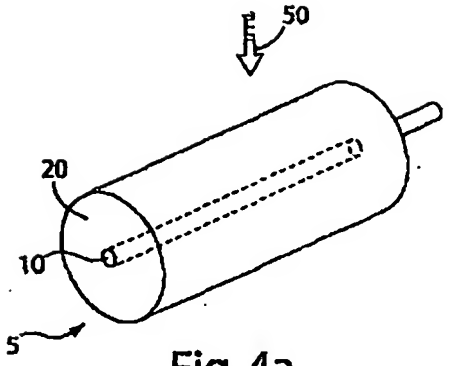


Fig. 4a

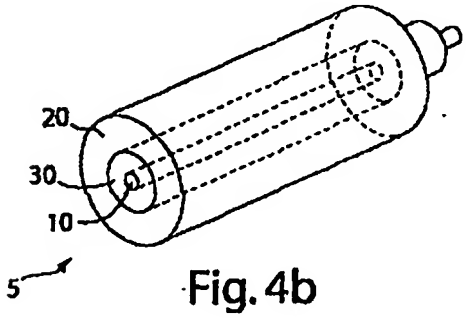


Fig. 4b

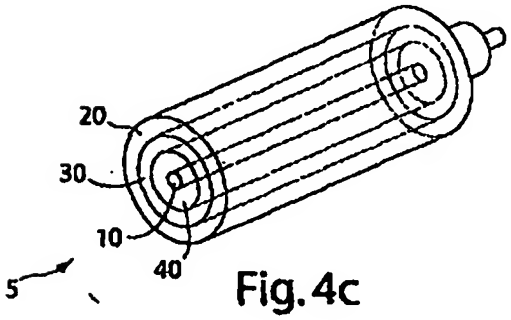


Fig. 4c

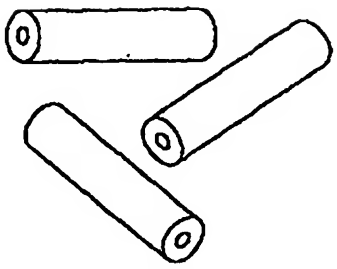


Fig. 5a

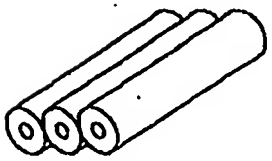


Fig. 5b

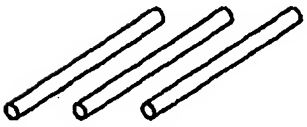


Fig. 5c

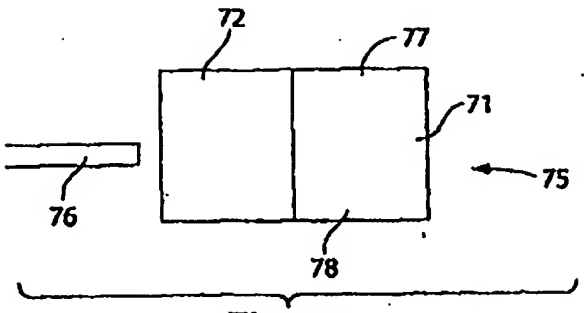


Fig. 6a

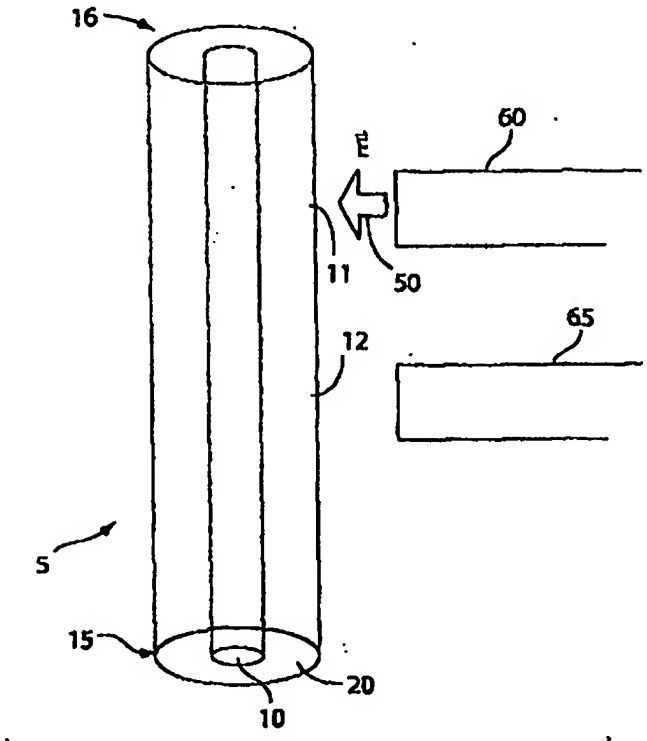


Fig. 6b

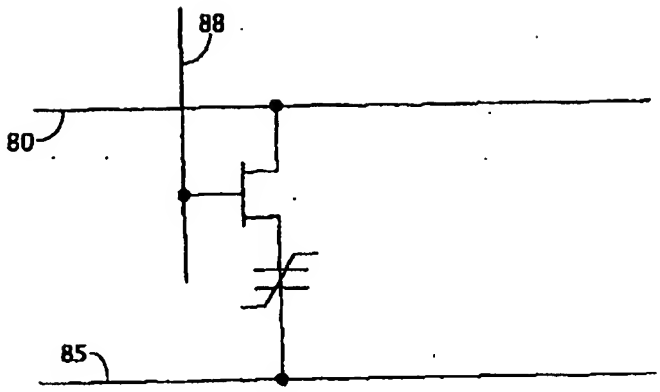


Fig. 7a

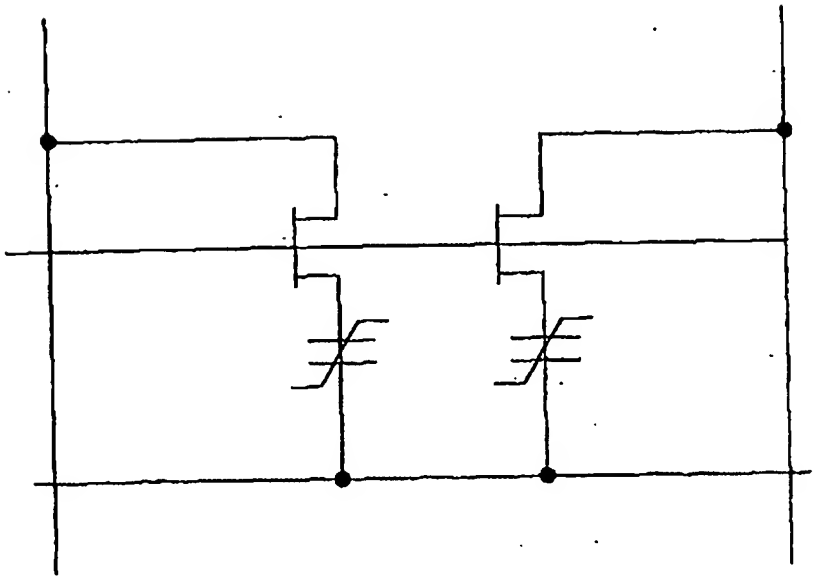


Fig. 7b

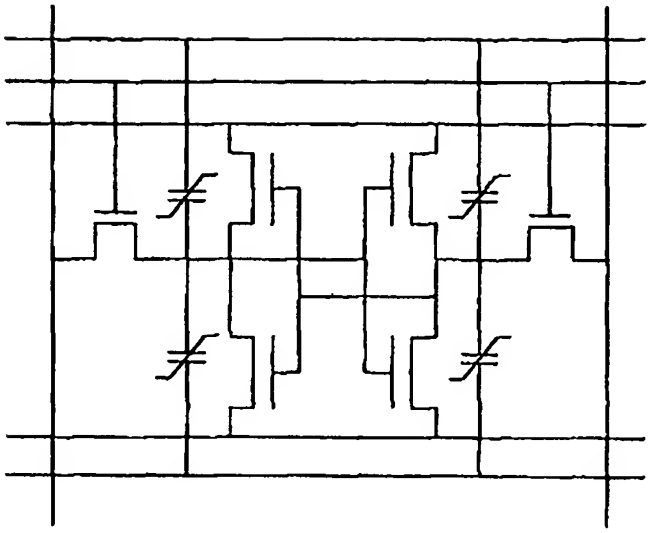


Fig. 7c

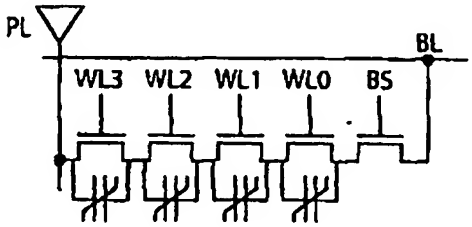
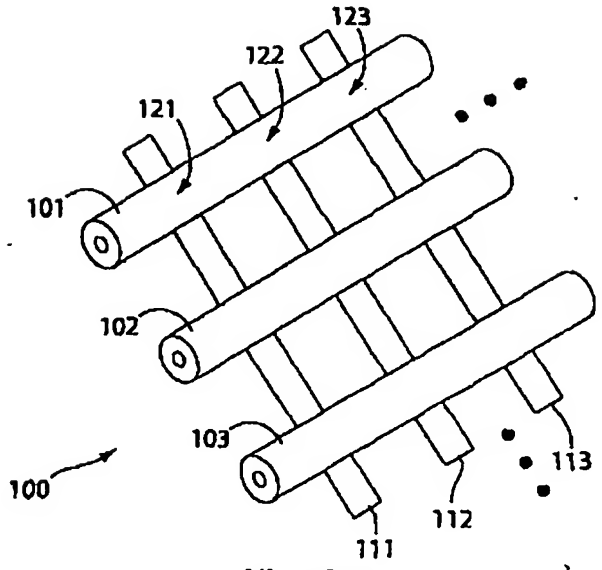


Fig. 7d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122
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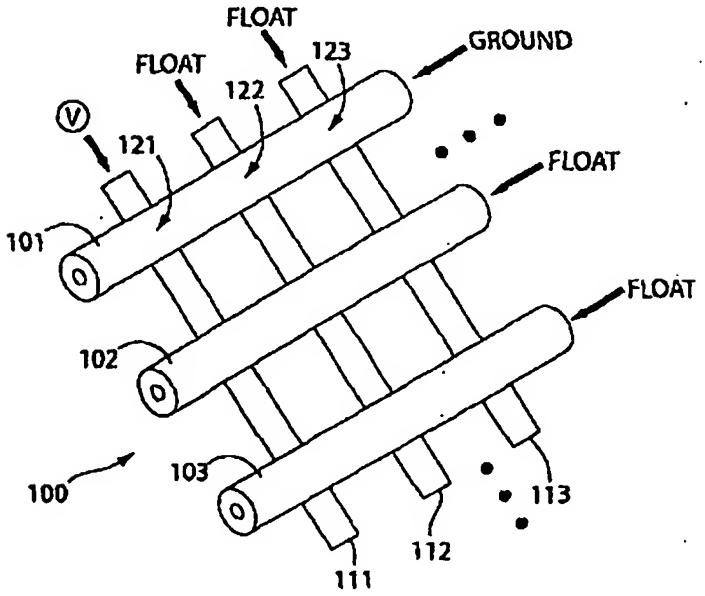
103
100
113
112
111

Fig. 8a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111

Fig. 8b

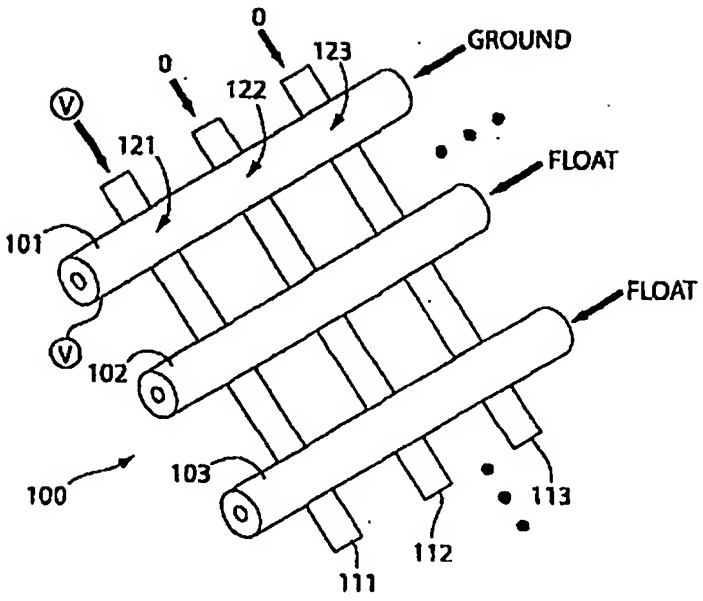
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Fig. 8C

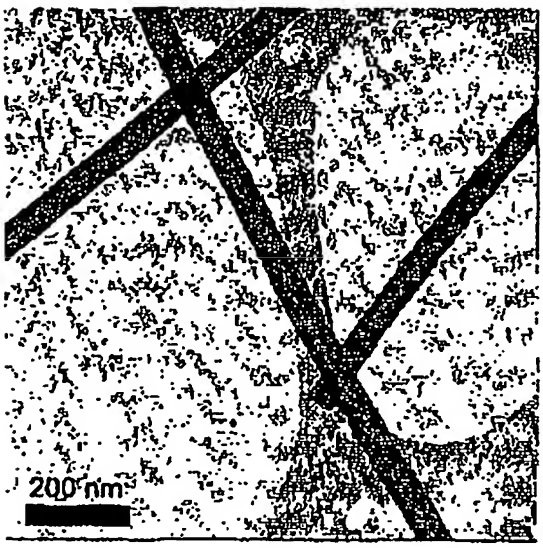


Fig. 9a

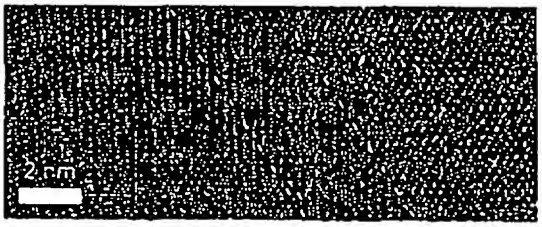


Fig. 9b

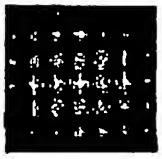


Fig. 9c

Fig. 9d

Fig. 9e

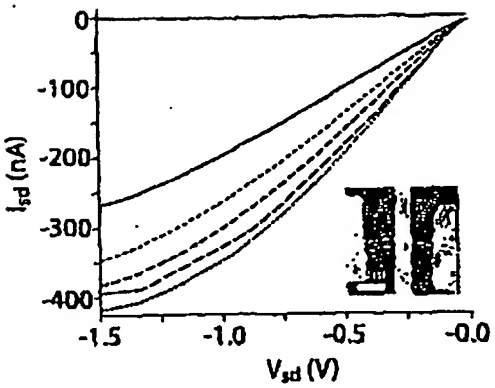


Fig. 10a

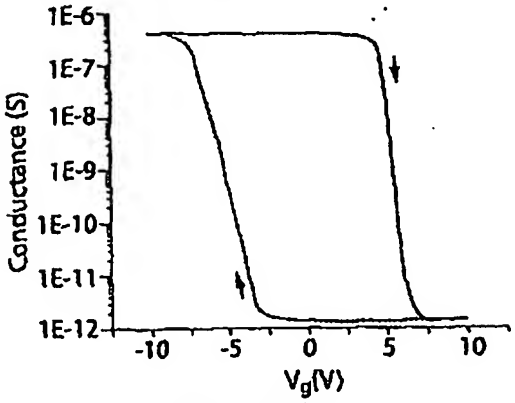


Fig. 10b

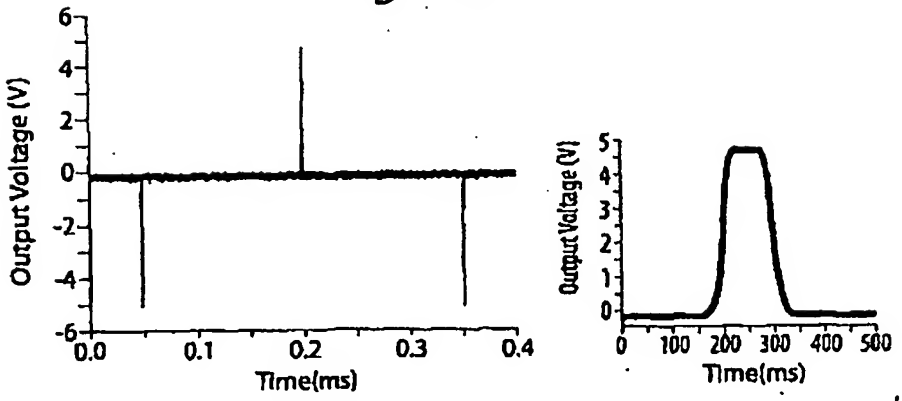


Fig. 10c

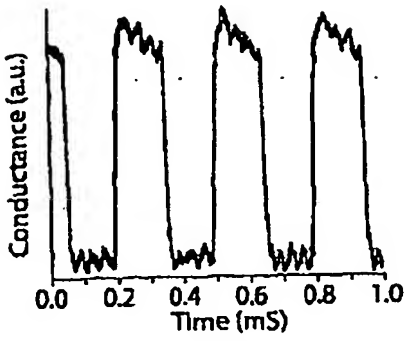


Fig. 10d

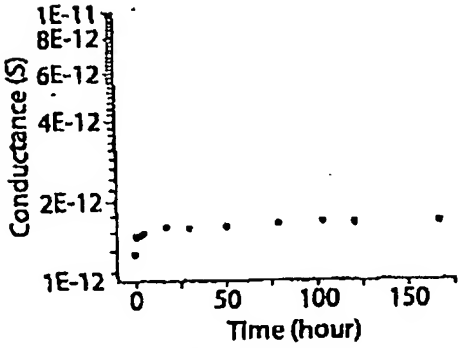


Fig. 10e

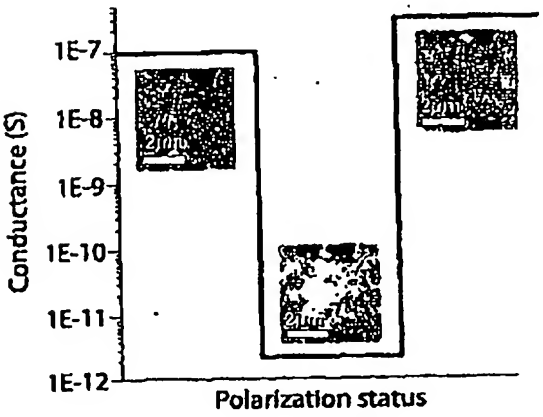
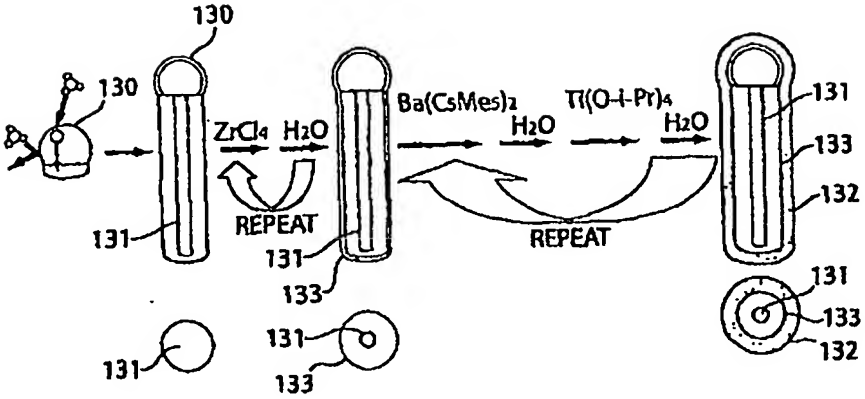


Fig. 10f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130
131
ZrCl4
H2O
REPEAT
131
133
Ba(CsMes)2
H2O
Ti(O-i-Pr)4
H2O
REPEAT
131
133
132
131
131
133
131
133
131
133
132

Fig. 11

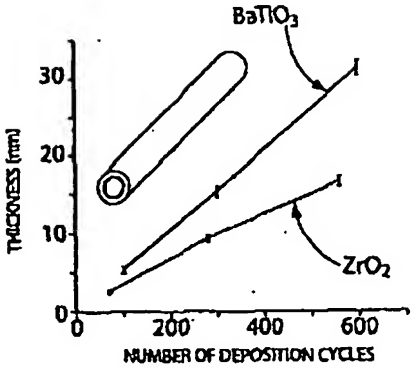

Fig. 12a

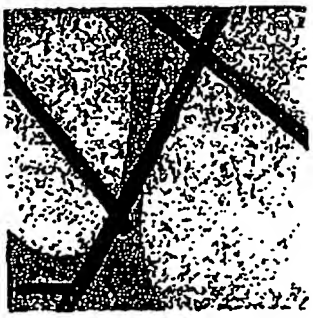

Fig. 12b

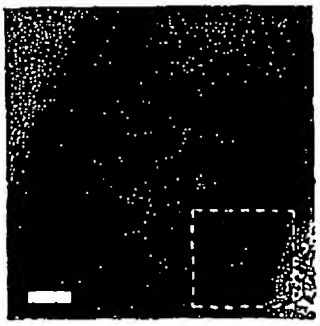

Fig. 12c

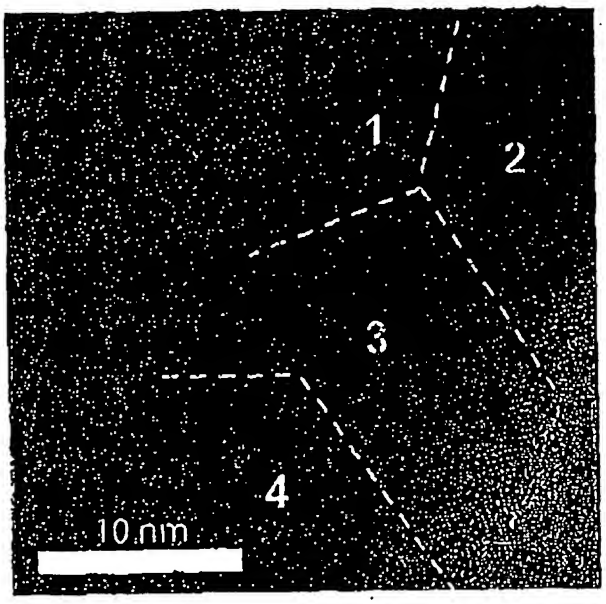

Fig. 12d

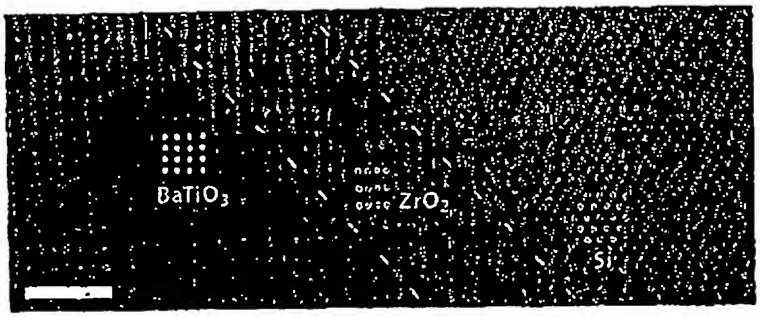

Fig. 12e

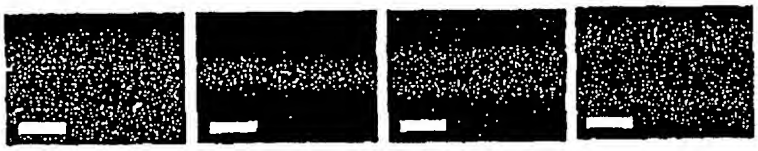

Fig. 12f Fig. 12g Fig. 12h Fig. 12i

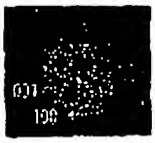

Fig. 12j

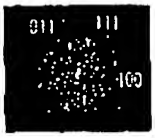

Fig. 12k

Fig. 12l

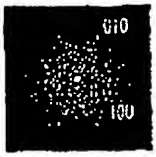

Fig. 12m

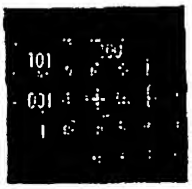

Fig. 13a

Fig. 13b

Fig. 13c

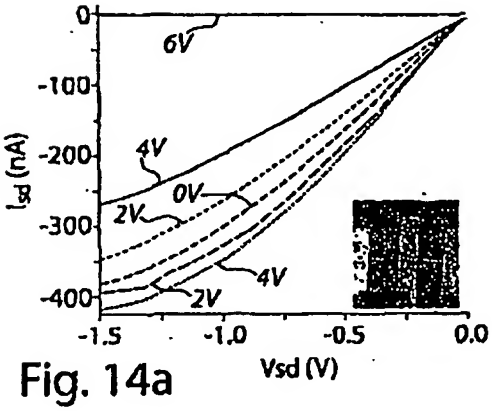

Fig. 14a

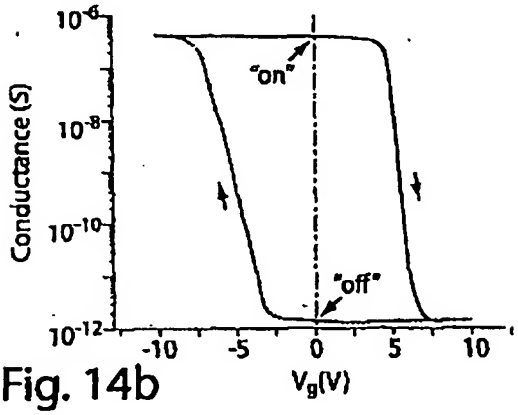

Fig. 14b

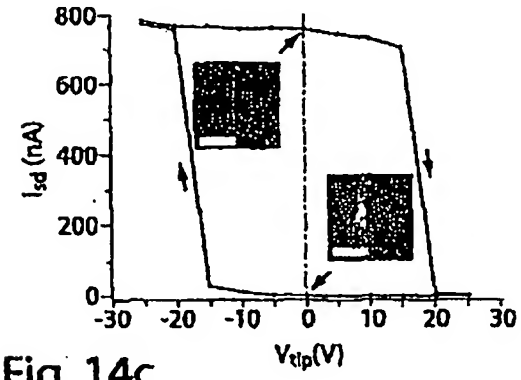

Fig. 14c

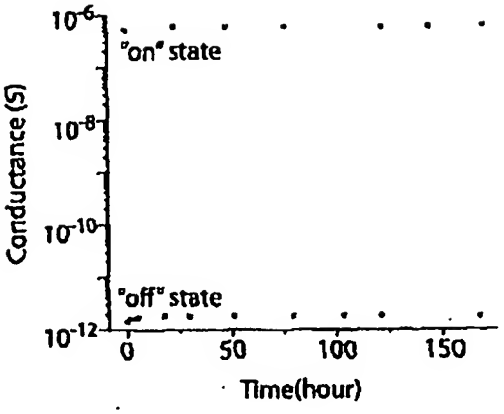

Fig. 14d

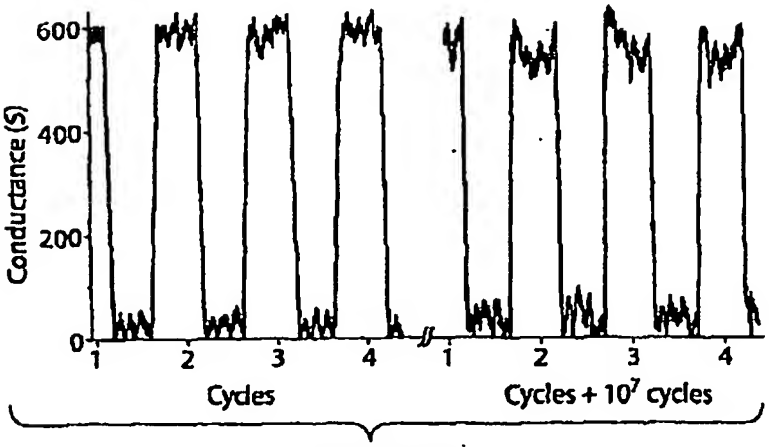

Fig. 14e

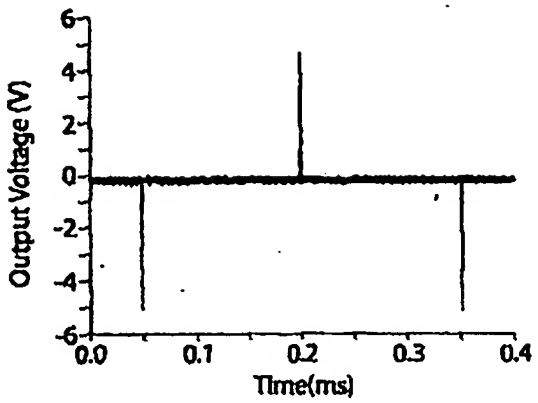

Fig. 14f

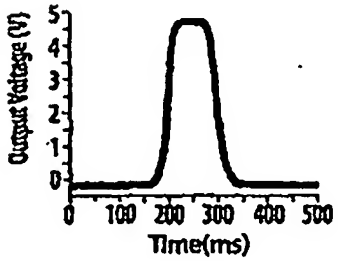

Fig. 14g

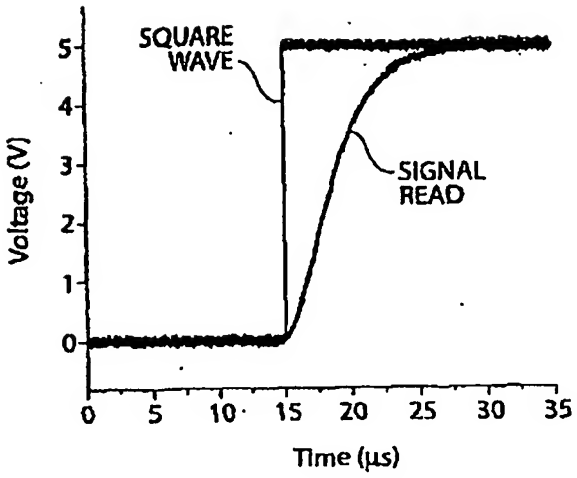

Fig. 15a

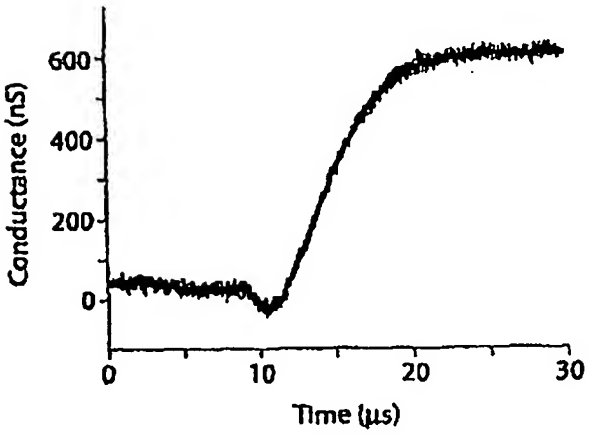

Fig. 15b

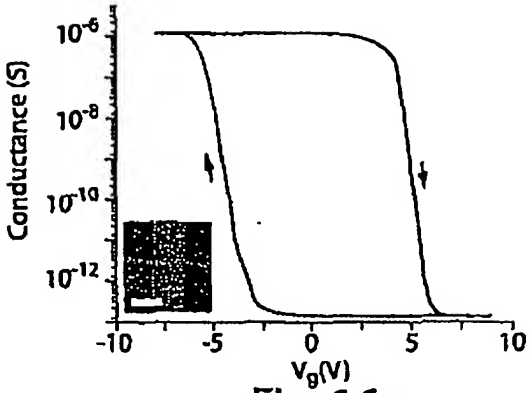

Fig. 16a

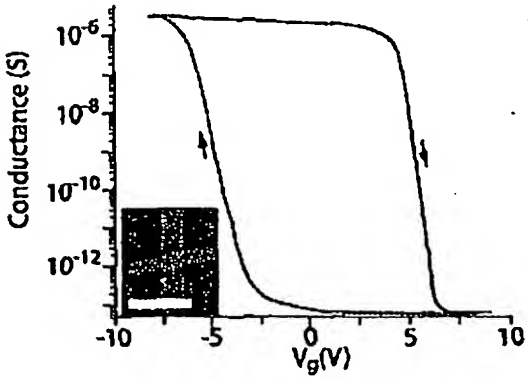

Fig. 16b

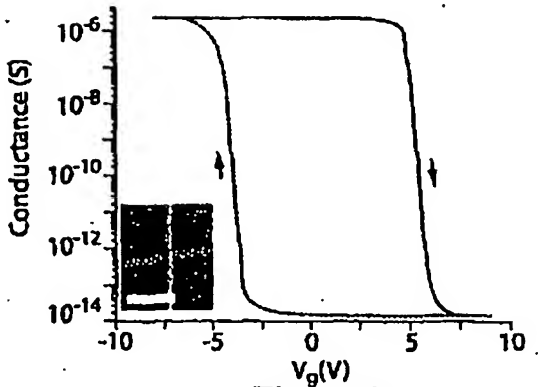

Fig. 16c

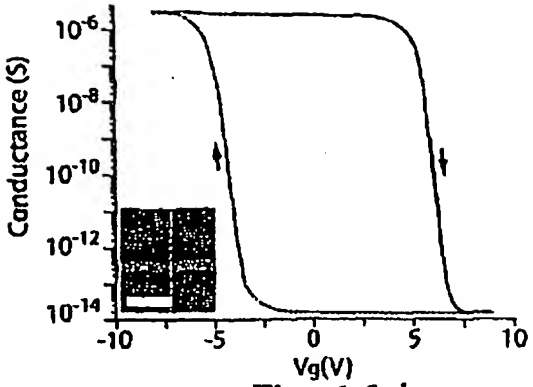

Fig. 16d

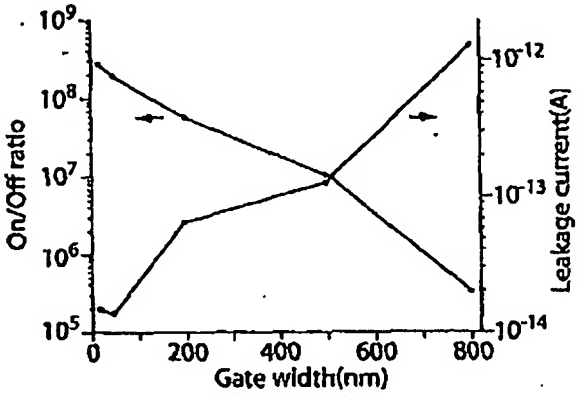

Fig. 16e

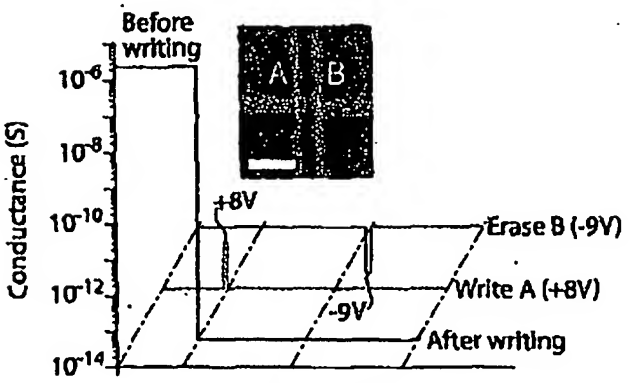

Fig. 16f

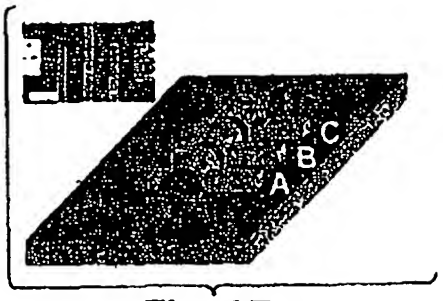

Fig. 17a

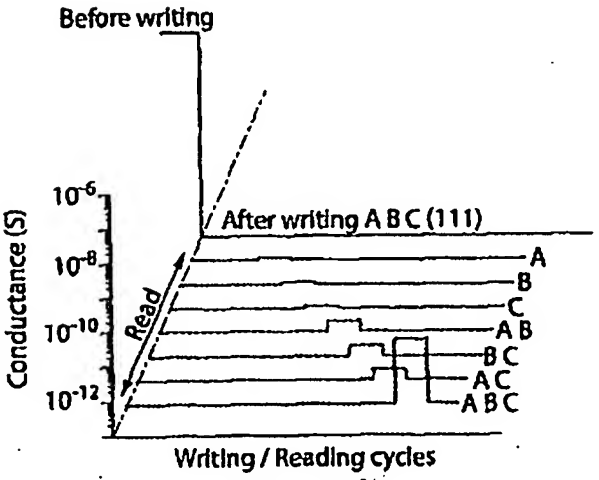

Fig. 17b

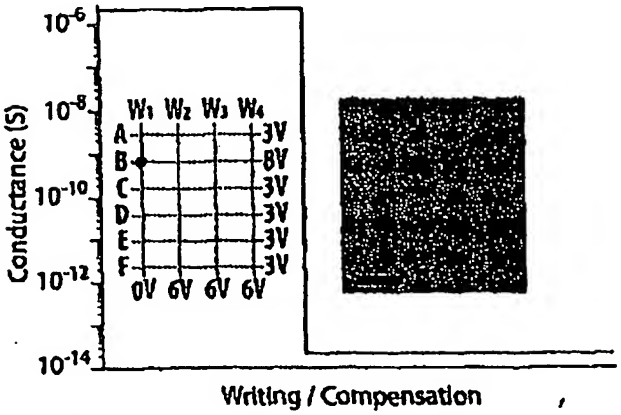

Fig. 17c

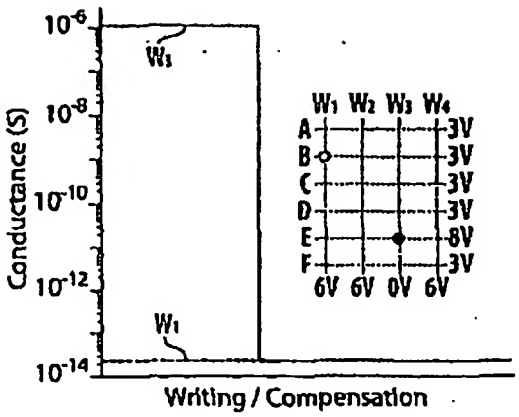

Fig. 17d

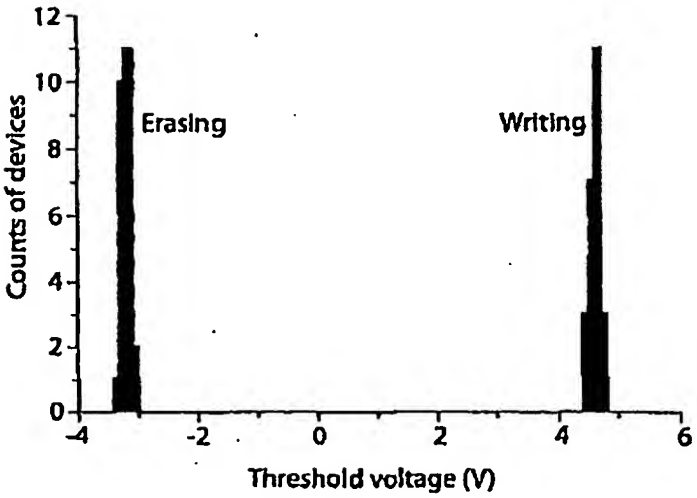

Fig. 17e